analog dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

Volume 22, Number 1, 1988

ANALOG DEVICES

Editor's Notes

WHAT IS "APPLICATION-SPECIFIC"?

To a casual reader of the trade press it must seem that the world has gone ASIC-happy. Certainly the ability to develop libraries of standard functional blocks and interconnect them on monolithic IC chips with a few swift strokes at the keyboard and a couple of passes with a mouse is an exciting prospect; it warrants a great deal of enthusiasm over potential savings of cost and space for both producers and customers. In fact, we at Analog Devices are looking forward to a major role in the high-performance application-specific IC market.

However, before a designer gets carried away with the idea that everything should be done this way and that you aren't really up with the state of the art unless designing a chip that will "do it all," it may be useful to consider what "application-specific" really means and the implications for the designer.

"Application," like "system," is an overused universal word that means different things to different people. To a user, an application-specific circuit is a purchased device or assembled collection of devices that can be used to maximize performance/cost for a given job; it may involve a home-grown kludge, a standard IC, a custom IC, a hybrid circuit, or even a module. In general, to a device manufacturer, an application-specific circuit can be a custom project for one user, a device intended for a specific role in a specific market (e.g., disk-drive data-recovery circuit), or a specialized device distinguished by function or performance—like a log amp or rms-to-dc converter.

Standard-cell-based custom ASICs have made their greatest inroads in digital circuitry, where low cost and turnaround time have become the norm. They are beginning to enter wide usage in some aspects of analog circuitry, typically in very-high-volume circuits with low-to-moderate performance and sophistication.

But high-performance analog and mixed-signal custom devices require something more: *the same kinds of processes, test capability, and design and applications expertise and experience that are needed to make high-performance general-purpose and application-specific ICs for the merchant market.*

Required processing capabilities include as a minimum the ability reliably to make low-drift references and high-input-impedance junction FETs; a combined bipolar-CMOS process to facilitate digital and analog signals on the same chip; a complementary-bipolar process to make possible high-speed analog circuits with excellent dc characteristics; and the ability to deposit precision resistors and laser-trim them. Also required are the design know-how to avoid the many pitfalls in predicting circuit behavior by simulation—and the experience in characterizing and testing linear ICs to insure the integrity of the product's performance.

There aren't many manufacturers of high-performance analog and interface ICs who have all of these capabilities, and there are even fewer who have manifested a serious interest in entering this market. That's why we're smiling.

Dan Sheingold

THE AUTHORS

Wyn Palmer (page 3 and page 8) is the engineering manager for disk-drive and video products at Analog Devices Semiconductor (ADS), which he joined in 1984. Earlier he had worked in the area of disk-drive design at DEC and Data General. He is a graduate of the University of Leeds, and the University of Southampton, in England. His accomplishments at ADS include the AD840 high-speed op-amp family, as well as the disk-drive and rms circuits described in these pages. He enjoys gardening and hi-fi.

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analog dialogue

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ISSN 0161—3626

DISK-READ ICs CONDITION AND DELIVER BITS AT 50 MBITS/s

AD890 Provides AGC Over Wide Range of Input Amplitudes

AD891's Precise Comparators and One-Shot Pinpoint Output Signal

by Wyn Palmer and Phil Carrier

The AD890 Precision Wideband Channel Processing Element* and AD891 Rigid-Disk Data Qualifier* are a pair of application-specific integrated circuits (ASICs) designed for use between the head readback preamplifier and data decoder of high-performance disk drives. Starting with the noise-corrupted and distorted signal from the disk head, these monolithic components produce error-free digital bits at rates up to and beyond 50 megabits/second (Mbits/s). With low-cost, user-provided reliable passive filters to shape the signal, the response of the *read*-channel circuitry can be matched to the data rate, the medium, and drive-mechanism characteristics.

The AD890 and AD891 remove a major impediment to realizing the potential of high performance drives in computer systems: the rate at which data bits can be recovered from the disk platter and passed on to the computer system. Increases in performance and capacity have been achieved by decreasing the track-to-track spacing, increasing the bit density within tracks, and using run-length-limited codes[1] that increase the amount of data represented by each group of flux reversals on the disk.

Until now, disk-*read* electronics, using either IC or discrete component designs, could accept data from the disk surface and reliably decode it into the original bits at maximum rates limited to 10-25 Mbit/s. However, with proper design, the interface between the drive and the computer bus is capable of much faster rates than the rate at which bits can be retrieved from the disk surface itself. The bus interface design is selected to match the disk capabilities and system needs, which range from lower-speed asynchronous designs to high speed, fully synchronous circuits. Any substantial improvement in overall data transfer speed has required significant improvements in the disk-read electronics, to avoid underutilizing the larger disk's capacity.

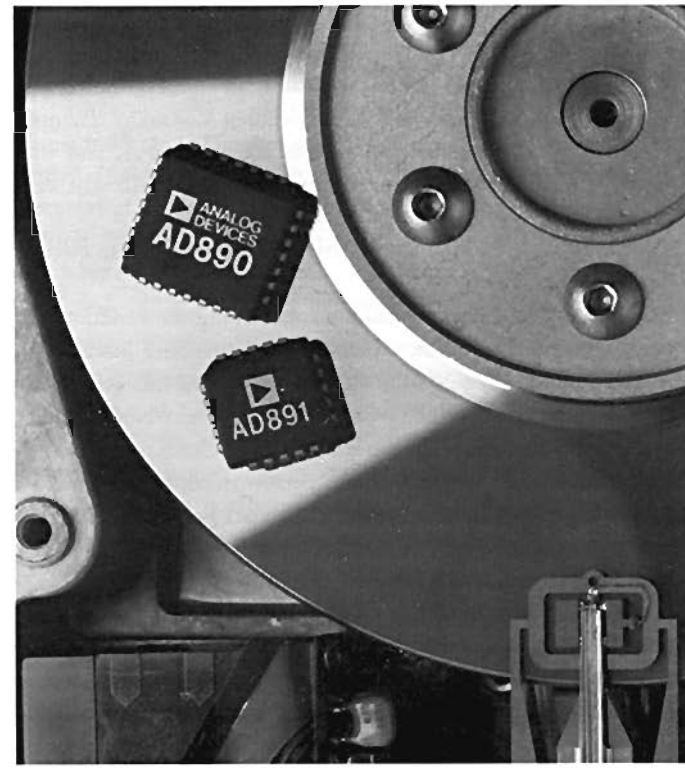
Extracting this data requires a combination of analog signal processing and digital circuitry. It is ironic that the original data bits were essentially ideal digital signals, and were stored to be used again as digital signals—but they must be recovered in the much more complex world of analog circuitry because of the non-ideal nature of the disk mechanism and magnetic data storage.

Though the physical distance between disk and head is small, the technical situation is analogous to a long-distance communications system that transfers data by radio or satellite from one continent to another, subject to varying noise and signal fading. Interestingly, the precision automatic gain control (AGC) developed for the AD890 *can also be used in non-disk-drive applications*, such as the front ends of communications receivers.

The disk-data-recovery circuitry needs to handle low-level, high-rate signals in a very unfavorable and noisy environment, and maximize the data transfer with acceptably low error rates. Uncorrected, raw bit error rates (BER) must typically be 1 in 10^{11} or

*Use the reply card for technical data on these devices.

[1]*EDN*, Mar. 31, 1987, "Run-Length-Limited Coding Increases Disk-Drive Capacity,"



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better despite these challenges:

- The signal from the disk head is small and noisy. Amplification boosts signal levels but can do nothing to improve the signal-to-noise ratio—may even make it worse.
- The signal level varies considerably (as much as 40 dB), depending on the instantaneous distance between the head and disk surface. This distance is continuously changing by small but significant amounts, as a result of mechanical tolerances and variations as the disk rotates.
- The shape of the signal from the Read head is not optimum for data recovery; it may change, depending on many factors. High-frequency spectral components are attenuated, and the signal spreads out in time, resulting in overlap with adjacent pulses (1's) or pulse-absences (0's).
- Temperature variations in the drive cabinet can cause circuit performance to drift.
- The timing of the data signals is not exact; minute variations in drive speed and mechanical eccentricities introduce jitter.
- At rates greater than 20 Mbits/s, recovering data bits reliably is always a challenge to the circuit designer, even when the data bits are relatively noise-free and stable. Propagation delays and phase shifts alone seriously affect performance; with temperature or time instabilities, the difficulties are compounded.

FUNCTIONS IN A DATA-RECOVERY SYSTEM

The functional blocks of the AD890 and AD891 are shown in Figure 1, along with typical signal waveforms at key points. Encoded binary signals are recorded as magnetic flux reversals; they occur at specific points in the medium. The output of the Read head is a band-limited voltage proportional to the derivative of the flux. The low-level signal from the Read head is amplified by an external preamplifier, located close to the head.

The preamp output goes to a critical element, a variable-gain amplifier (VGA). This amplifier provides continuously variable gain or attenuation over a wide range of 40 dB, depending on the signal level, controlled to produce an output at precisely the level required for optimum operation of the subsequent filters and comparators that make the 1-or-0 data-bit decision. The control signal for the VGA comes from an automatic gain control (AGC) circuit, a feedback loop that measures the output, compares it with the desired level, and continously adjusts the gain of the VGA to maintain the desired output level.

An amplified and properly leveled signal from the Read head is not yet ready to be decoded into error-free 1's and 0's. Accordingly, the *read*-head signal from the VGA goes through filtering and gain stages, including gain-of-4 buffers. The purpose of low-pass filtering and equalization is to shape the signal amplitude and phase spectra to compensate for distortion, phase shifts, and nonlinearities in the data -writing and -reading processes (e.g., head coil inductance, mechanical arm resonances).

The design of these intermediate filters is quite critical to the specific application and must be done by the drive manufacturer based on the characteristics of the particular disk technology and head design employed. This represents, in effect, the value that must be added by the manufacturer to achieve low error rates through proper equalization-filter design[2].

The signal from the buffer and filter stages is used in two ways: it goes to the AGC circuit as part of the closed-loop level control, and it continues through the signal processing chain for extraction of the actual binary data.

The AGC circuit has a full-wave rectifier to measure the output of the VGA and derive an output proportional to the average deviation. The rectifier output is subtracted from a reference—or amplitude set-point—and integrated; the result is applied to an exponential function, then multiplied by the input to control the VGA gain. The integrator provides filtering and insures zero average error in the steady state, and the exponential factor is used so that steady-state integrator output increments correspond to equal *percentage* changes of input rather than to the actual wide-ranging magnitude of change.

The attack and decay rates at which the AGC changes gain in response to signal amplitude changes must be matched to the application to keep the response from being either too slow (inadequate gain tracking) or too fast (instability and gain "pumping"); this is accomplished with an external capacitor that adjusts the integration time constant.

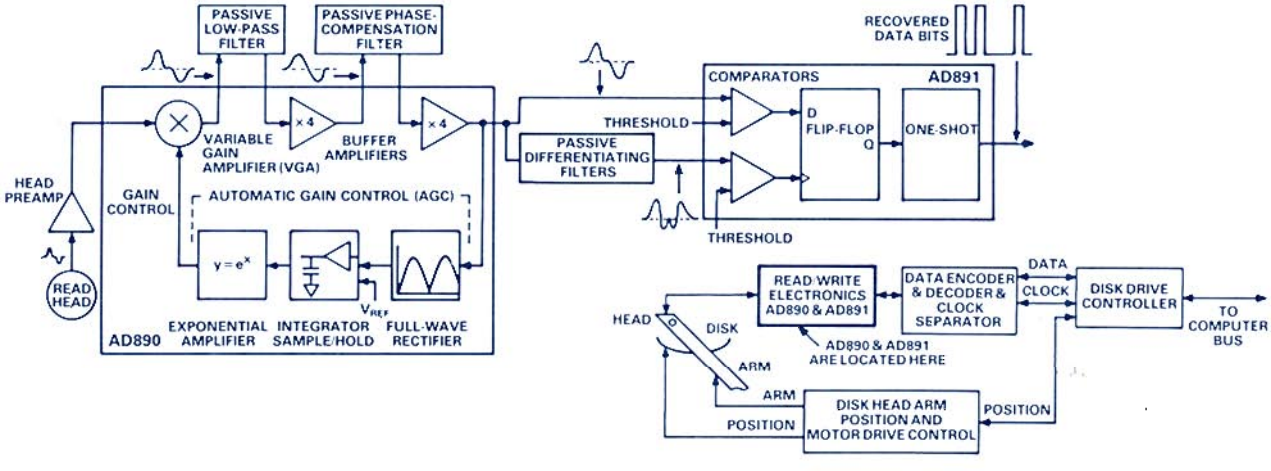


Figure 1. Disk output bit-recovery system. Simplified diagram shows chip functions, auxiliary filter circuitry, and waveforms at key points.

[2] *Hewlett-Packard Journal*, January, 1984, "Second-Generation Disc Read/Write Electronics."

After the filtering and equalization, the data is ready to be extracted. The signal is differentiated to locate the peaks (zero crossings of the derivative); when the derivative of the signal is at zero, the signal waveform should be compared to the "valid signal" threshold (Figure 2a - 2c). Both the original signal and the differentiated signal are passed to threshold comparators.

The threshold level is set low enough to qualify valid pulses, but high enough to ignore noise. The amplitude comparator output goes to a D-type flip-flop clocked by the derivative comparator; a flip-flop output transition corresponds to a data bit; (a one-shot resets the flip flop shortly thereafter). The flip-flop transition drives a one-shot that finally produces data output pulses of precise width. These pulses are accurate counterparts of the data bits originally recorded on the disk surface; they can be decoded and error-corrected using standard high-speed digital circuitry. The one-shot's stability is critical at these high rates since even slight drift or jitter can look like false bits and lead to errors in the decoder and timing-recovery circuitry of the disk controller.

A useful data recovery circuit needs some additional features. To avoid saturation by the high-level Write fields, an input clamp is applied to the *read* circuit when writing to the disk by reducing the impedance of the input stage to a very low value; at the same time, the integrator can be switched to a *hold* mode to preserve the value of gain. This minimizes disturbance to the AGC and VGA and assists in producing a rapid recovery after *write/read* switching. The ability to externally set VGA gain is also useful in test and for specific application modes.

DESIGN AND PERFORMANCE OF THE AD890

The key to the design and performance of the AD890 Precision, Wideband, Channel Processing Element is a 4-GHz FLASH bipolar process that uses double-level metallization and laser-trimmed thin-film resistors (Figure 3). This combination provides stable and predictable currents in bias circuits, and the ability to compensate for temperature variations in gain and comparator offset. Bandgap voltage references provide the required stability. When operating at 50 Mbits/s and higher rates, achieving high performance depends as much on stability, predictability, and low jitter as on such traditional parameters as noise, bandwidth, and maximum slew rates.

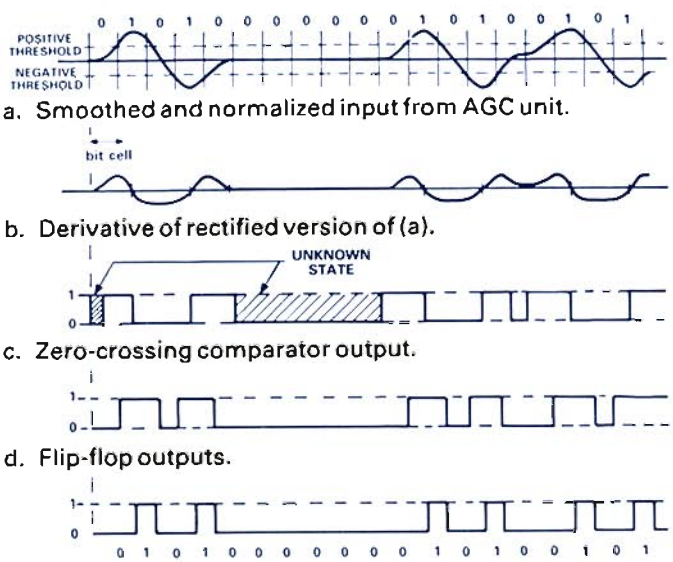


Figure 2. Data qualifier examines signal level at time of waveform peak to determine if valid bits are present.

The AD890 is essentially a precise 100-MHz AGC with up to 40 dB of gain-control range (+30, −10). The r-f path is fully differential for optimal high-frequency performance and minimal distortion. Three gain cells are provided: a 30-dB (nominal maximum) variable-gain block, and two 12.75-dB buffers. The two buffer stages simplify the low-pass filter and equalizer design.

The outputs of the gain stages are emitter followers capable of driving 200-ohm differential networks. The variable-gain amplifier's full-scale gain setting is trimmed to 30 dB ±0.6 dB and remains within 0.25 dB of nominal over the full operating temperature range. Wideband gain is maintained to within 1 dB of nominal at 50 MHz, at gains up to 26 dB below full-scale gain setting. Together, these three gain cells offer the best performance available in monolithic designs for this application.

As an AGC, the AD890's essentially single-time-constant feedback loop provides highly predictable attack and decay characteristics in response to input steps. With an external integrating capacitance of 1,000 pF connected, attack and decay times are about 1μs. The low-to-high and high-to-low gain transients are essentially identical, and independent of the initial gain setting, thus providing a nearly ideal AGC action (Figure 4). The single pole also ensures no overshoot or ringing. The AGC characteristics are gain-compensated so as to make the settling time essentially independent of transient magnitude.

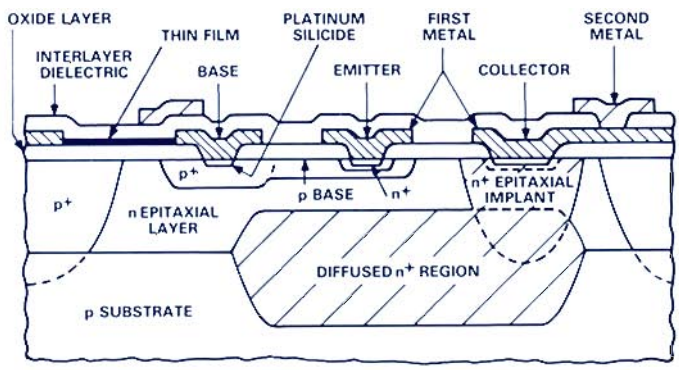


Figure 3. Cross section of FLASH-process die showing two-level metallization and laser-trimmed thin-film resistors.

In the AGC gain-setting section, the full-wave rectifier has 100-MHz bandwidth; for accuracy, its dc offset is trimmed to less than 10 mV in manufacturing. The full-wave rectifier design allows easy, accurate amplitude detection of signals intended to provide servo positioning information to the disk arm. A single external capacitor can adjust the peak-to-average ratio of the full-wave rectifier. The rectifier output and a precision reference voltage are differenced in an averaging, high gain integrator-sample/ hold circuit for accurate AGC operation. A second full-wave rectifier in the AD890 can be used to generate a threshold output used for creating a data qualification level.

The gain acquired during AGC can be "held" (set via control lines) to minimize signal degradation during data regions. When in *hold* mode, the decay rate for the AGC is about 0.2 dB per ms, or about 0.02 dB for an average 100-μs sector length, a gain change of less than 0.2%. As an alternative approach—and for test purposes—the AD890 can be used in a mode selected by the control lines, not as an AGC, but as a very accurate programmable

gain amplifier with 55.5 dB of VGA and buffer gain with 0 V on the gain control pin, and a gain-reduction rate of 1 dB for each 20-mV decrease in the control voltage. Performance is trimmed and temperature-compensated.

The variable-gain amplifier has an equivalent input noise figure of only 5 nV/$\sqrt{\text{Hz}}$, while the "gain of 4" buffers have a noise figure of 7 nV/$\sqrt{\text{Hz}}$. The AGC control is linear to within ±0.5 dB over a 26-dB AGC range for the full bandwidth, and has excellent performance to 40 dB of range, Figure 5. Its fast and clean response to an input step can be seen in Figure 4.

Another critical feature is the input clamp, operated during data writes to the disk. When the clamp is activated (via the mode control lines), the input impedance of the amplifier falls to about 8 ohms, greatly reducing the input resistance/coupling capacitance time constant. Also, with 200 Ω || 0.1μF source impedance driving the input (a typical source value), differential input signals are attenuated by more than 34 dB. This greatly assists in producing a rapid recovery after *read/write* switching.

DESIGN AND PERFORMANCE OF THE AD891

The AD891 is basically a very fast, single-bit a/d converter, which provides output pulses corresponding to zero-crossing events of sufficient magnitude to exceed a threshold value. It is fabricated in temperature-compensated reduced-swing ECL, which exhibits typical propagation delays of 0.6 ns per gate. The output's ECL data pulse has standard 10KH ECL logic levels. It can drive a 75-ohm transmission line, if properly terminated.

The signal from the AD890 arrives through a second-order discrete-delay-line and differentiator, which is made of passive components and provides identical time delays through both the undifferentiated and differentiated data paths. This scheme permits the signal amplitude to be qualified at the zero-crossing time. The second-order design also provides uniform magnitude and phase-delay/group-delay characteristics, up to about 60% of the resonant frequency. This minimizes dispersion of the processed readback data coming from the AD890 and prevents degradation in error rates. The 2nd-order section also provides a high-frequency rolloff, useful in rejecting high-frequency noise.

This design qualifies the pulse by both level and time. Level qualification is performed on alternating half cycles of the data waveform via a user-defined threshold level, applied to a pair of ultra-fast comparators with 3-ns propagation delays (only one

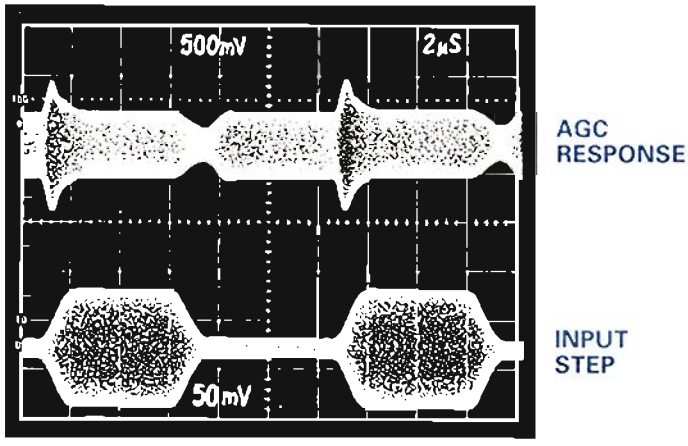


Figure 4. Response of AGC to step input.

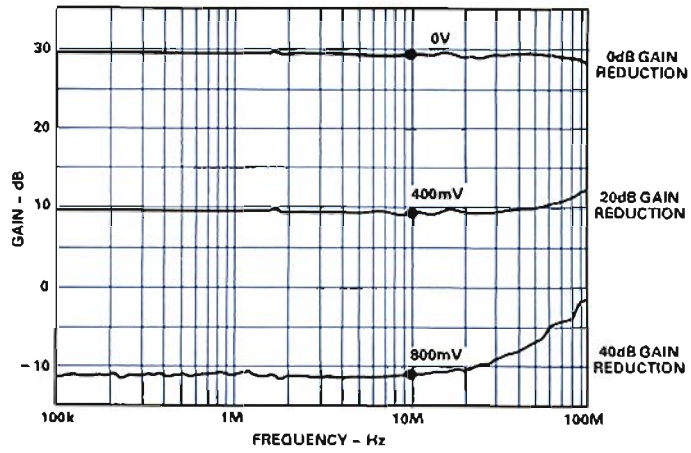


Figure 5. VGA gain versus frequency as a function of control voltage – showing linear 20 dB/400-mV gain sensitivity.

shown in Figure 1—the upper one), matched to better than 300 ps. A third comparator (the lower one in Figure 1), for derivative zero-crossing detection, provides the time qualification.

Since a comparator with significant offset will produce a double pulse ("pulse pairing") in real waveforms with non-infinite slew rates, the offsets of the comparators in the AD891 are trimmed to less than 250μV to minimize this error source. The offset and delay characteristics of the comparators are carefully controlled to remain constant over temperature; a bandgap reference provides temperature stability. The timing error contributed by the AD891 from offset, gain, and drift is less than 1 nanosecond.

The outputs from the amplitude qualification comparators are applied to the "D" inputs of two master-slave flip-flops (one shown in Figure 1), clocked by the outputs from the zero crossing detector/comparator. Each valid zero-crossing event causes a one-shot—with a user-definable period—to be triggered. This delays resetting of the flip-flops, preventing detection of additional zero-crossing events until the one-shot period ends. Simultaneously, an output one-shot is activated; its leading edge is synchronous with the change in D-flop outputs.

The user-definable period of this one shot is intended to insure adequate output-pulse duration for transmission to the users' data decoder. The period of each one-shot, ranging from 5.4 ns to 180 ns, is set by a single resistor; all the one-shots are trimmed to ensure predictable settling of the pulse periods. The final output of the IC is a 10KH ECL-compatible pulse, which corresponds to the detected zero-crossing, with a 7-ns delay.

Both units require ±5-volt power and dissipate less than 500 mW. For operation on +5- and +12-volt power, only five resistors and one diode are needed: four resistors for level-shifting the TTL mode control lines, and one resistor and a diode to reduce internal power dissipation under maximum operating voltage conditions. The AD890 is housed in a 24-pin Cerdip package or 28-pin plastic leadless chip carrier (PLCC), while the AD891 is available in either 14-pin Cerdip or a 20-pin PLCC. Price of each drops to well below $10 in quantities of 10,000. ◘

PRECISION BIPOLAR OP AMP HAS LOWEST OFFSET, DRIFT

AD707 Series Has max Offsets & Drifts as Low as 15 μV, 0.1 μV/°C
Open-Loop Gain is typically 13 V/μV with CMR of 140 dB

The AD707 op-amp* sets a new standard among high-dc-precision devices for designers who require low input offset voltage and drift, low noise, high open-loop gain, and high common-mode rejection. The highest performance grade, AD707C, with less than 15-μV offset, is the first bipolar monolithic op amp specified to have offset voltage drift below 0.1 μV/°C. Its dc accuracy specifications are comparable to those of chopper-stabilized amplifiers, but with less noise and far lower cost.

Higher accuracy and precision benefit the designer by tighter error budgets at lower cost through the elimination of offset trim components and the associated time required for trimming. Even the lower-cost, relaxed-spec grades, AD707J and AD707K, provide significant performance improvements over industry-standard op amps: the AD707J has typical input offset voltage of 30 μV with drift of 0.3 μV/°C; for the AD707K (best price/performance choice), offset is 10 μV, with 0.1 μV/°C drift.

The high open-loop gain (8 V/μV min and typically 13 V/μV) and 140-dB typical common-mode rejection (CMR) of the AD707C make it ideal for applications such as precision instrumentation amplifiers. This open-loop gain is maintained over the *full 10-V output range when driving a 1,000-ohm load*. As shown in Figure 1, the gain and gain linearity are better over the output range than for comparable industry-standard op amps.

Open-loop gain and phase shift as a function of frequency are shown in Figure 2. Unity gain occurs at 0.9 MHz, with a phase margin—the difference between the measured phase shift and 180° at the unity-gain frequency—of 58°.

Offset current for most grades drifts less than 1 pA/°C, while the input bias current has a maximum value of 1 nA for the C-grade device. Power supply rejection (PSR) is at least 120 dB—and is typically 10 dB greater than that minimum figure.

Noise is a critical parameter for dc precision op amps; both low-frequency and wideband noise are specified. Input voltage noise in the 0.1 to 10 Hz band is 0.35 μV peak-to-peak (max-

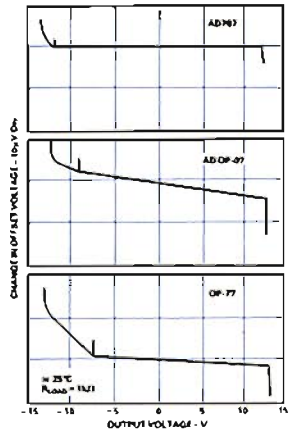
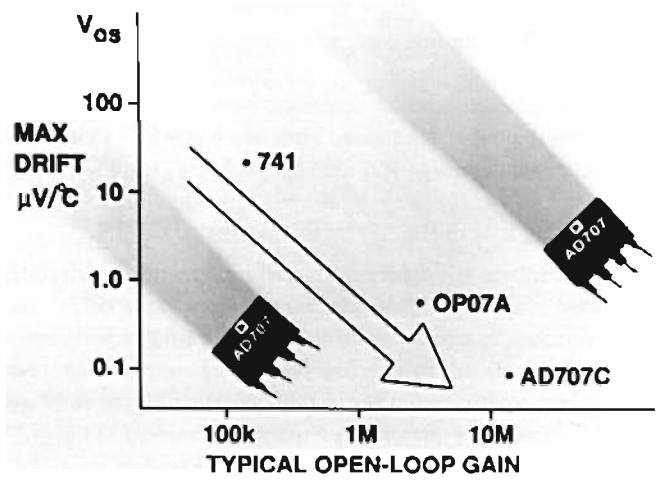


Figure 1. Linearity error of the AD707 and other precision dc op amps (ADI test results).

*For technical data, use the reply card.



imum), guaranteed by test; at 1 kHz, the noise spectral density is less than 11 nV/$\sqrt{Hz}$. Input current-noise spectral density is typically 0.12 pA/$\sqrt{Hz}$ (0.17 nA/$\sqrt{Hz}$, max) at 1 kHz.

Output impedance of the AD707 series is low: for closed-loop gain of +1, it is essentially a 5 μH inductance (1 mΩ at 33 Hz, 1 Ω at 33 kHz) and, for gain of 1,000, it is essentially 5 mH in parallel with 30 ohms (1 Ω at 33 Hz). With a 10-kΩ load, the output can swing to within 1 volt of positive and negative rail for power supplies from ±3 V to ±22 V.

For a dc-optimized op amp, the AD707 is surprisingly fast. The closed-loop bandwidth of the AD707 (unity gain) is at minimum 0.5 MHz, and typically 0.9 MHz. It can settle to 18 bits within 100 μs, with a typical slew rate greater than 0.3 V/μs.

The AD707 family is available in 7 performance grades and several packages: 8-pin plastic mini-DIP, small outline, hermetic Cerdip, and hermetic TO-99 metal cans, for temperature ranges of 0 to +70°C, −40 to +85°C, and −55 to +125°C. S- and T-grade devices are available processed to MIL-STD-883B, Rev. C. Prices (100s) begin at $1.25/$3.25/$16 (AD707JN/KR/CQ).

The AD707 family was designed by Moshe Gerstenhaber, at Analog Devices Semiconductor, Wilmington, MA.

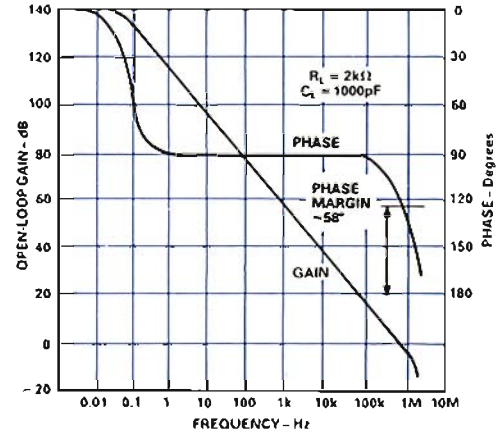


Figure 2. Open-loop gain and phase versus frequency

LOW-COST TRUE-RMS CHIPS ALSO COMPUTE AC AVERAGE

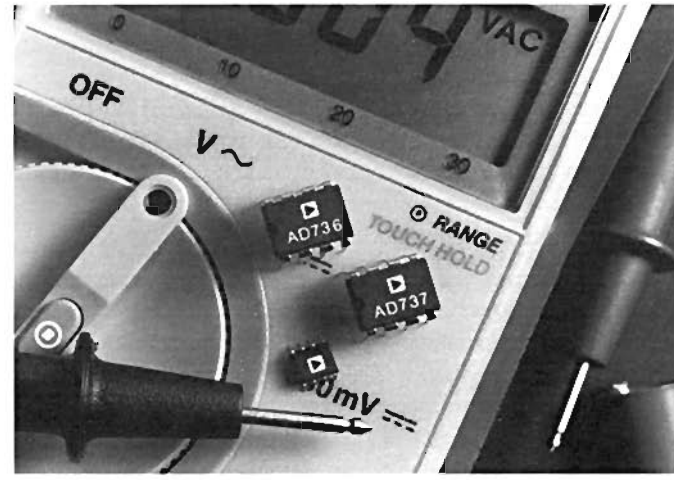
Measure 200-mV-RMS LF & Audio Signals with 100-μV Resolution

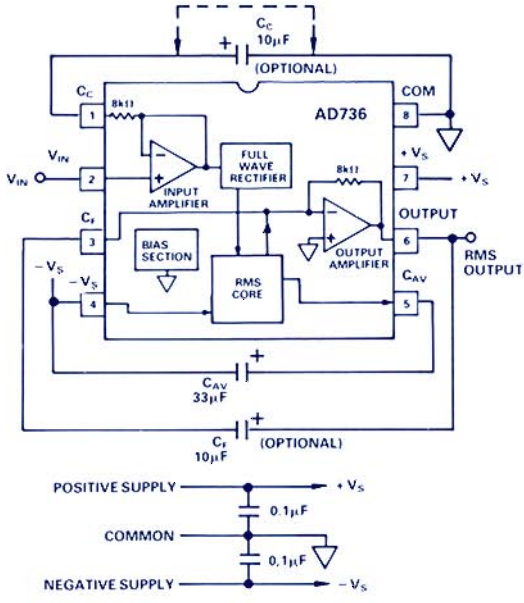
AD736 Has Buffered Voltage Output; AD737 Saves Battery Power

by Chuck Kitchin, Will Drachler, and Wyn Palmer

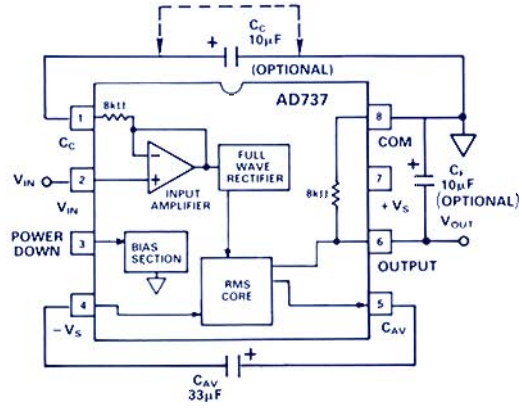
The AD736* and AD737* are flexible new monolithic rms-to-dc converters combining low cost, small size, and low power drain. They replace discrete designs, saving board space and assembly cost in multimeter, audio, automatic-gain-control, and many portable-equipment applications. They are housed in a choice of 8-pin plastic small-outline and minidip packages, for 0°C to 70°C grades—and in Cerdip for −40 to +85°C grades. Prices start at $3.58 in 100s for both the AD736JN and the AD737JN.

They are members of a family of monolithic rms-to-dc converters that started with the AD536 (*Analog Dialogue* 11-2, 1977). The AD736 is a complete low-impedance-voltage-output device, while the AD737—designed for very low power-drain applications—has a power-down control input for standby currents as low as 40 μA maximum, and it omits the output buffer amplifier. Even without this feature, both devices require little quiescent power, 200 and 160 μA (AD736 and AD737) with ±5-volt supplies.





a. The AD736, shown here connected for true rms, has a buffered output.



b. The AD737 omits the output buffer, has power-down control to minimize drain on power supply.

Figure 1. RMS-to-dc converter block diagrams.

*Use the reply card for technical data

Depending on how they are connected, these devices will compute either mean absolute-value, root mean-square, or instantaneous absolute-value measures of an ac or dc input voltage:

$$\frac{1}{T}\int_{-T/2}^{+T/2}|y(t)|dt \quad \text{or} \quad \sqrt{\frac{1}{T}\int_{-T/2}^{+T/2}y(t)^2\,dt} \quad \text{or} \quad |y(t)|$$

HOW THEY WORK

RMS is a direct measure of the power or heating value of an ac voltage: if an ac (or ac + dc) signal of any peak value and shape has an rms value of 1 volt, it will produce the same amount of heat in an R-ohm resistive load as will 1 volt of steady dc voltage. In this sense, rms is a universal measure of a signal. Some excellent wideband rms measuring units have been built that use the heating effect; however, it does not stack up as a good general-purpose approach for practical low-power, low-cost, wide-dynamic-range IC measuring devices.

Analog Devices rms-to-dc converters† solve the rms equation by analog computing; that is, they continuously produce the absolute value of the signal to be measured, square its magnitude, then take the average and square-root it. Since the measurement is performed continuously, an averaging (low-pass) filter is used to approximate continuous averaging instead of computing the definite integral indicated above. The time constant of of the filter is established *by the user*—with externally connected capacitance—to serve the needs of the application.

Figure 1a illustrates the process. An input buffer amplifier provides a choice between a high-impedance (FET) buffered input

†For further information on root-mean-square advantages, concepts and devices, see *RMS-to-DC Conversion Application Guide*, 2nd edition (1986) available from Analog Devices FREE upon request—and ADI's classic: *Nonlinear Circuits Handbook* (1974), $5.95.]

and a lower-impedance (8-kΩ) input having wider dynamic range and bandwidth. The signal is full-wave rectified and applied to an "rms core," which consists of a set of logarithmic diodes in a temperature-compensated configuration; they perform the squaring and square-rooting. Terminals are furnished for connection to the averaging capacitor, C_{AV}. Output (AD736) is via a buffer op amp, with provision for an optional external feedback capacitor, C_F, which can provide additional filtering in the rms mode and basic filtering in the full-wave-rectifier mode.

If C_{AV} is not connected, the computation is in effect the square root of the square of the absolute value of the input—which in the ideal case is simply equal to the absolute value of the input. With no capacitors, the output is the unfiltered instant-by instant absolute value; but with feedback capacitor, C_F, connected, the device measures the *mean* absolute value (average rectified value).

If the measurement is a purely "ac" measurement, i.e., if it must ignore the average (or dc) level of the input waveform, the input may be capacitively coupled. When the high-impedance "+" input is used, connect an optional ac-coupling capacitance, C_C, from pin 1 to ground to eliminate errors due to input offset and drift, insuring a resolution of 100 μV or better.

Figure 1b shows the basic circuitry of the AD737 connected for true-rms computation. It is similar to the AD736, except that its output is brought out at low level across an 8-kΩ source resistance (in parallel with the optional external filter capacitance, C_F).

HOW WELL DO THEY WORK?

The general-purpose AD736 is internally laser trimmed to an accuracy of ±0.5 mV ± 0.5% of reading max in the low cost J/A grades (±0.3 mV ± 0.3% rdg max K/B grades) including its output buffer amplifier. The AD737, optimized for portable meters, omits the buffer amplifier, reducing these errors to ±0.4 mV ± 0.5% of rdg (±0.2 mV ± 0.3% rdg). These sets of specs are for 1-kHz sine waves. Both chips will operate over a wide range of supply voltage: from ±3 volts up to ± 16.5 volts.

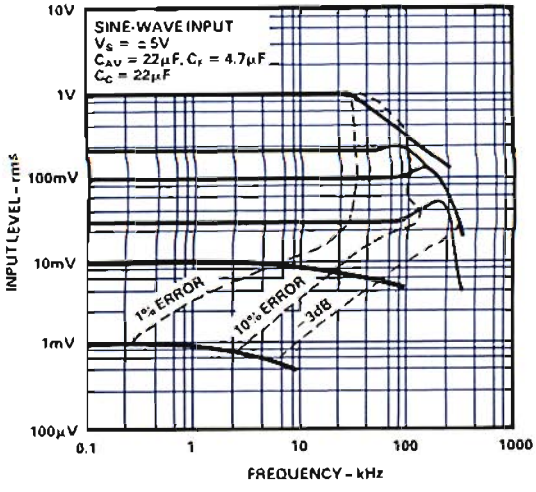


Figure 2. Frequency response, driving high-impedance input (pin 2). Flat response (to beyond 100 kHz at higher amplitudes) is available when low-impedance pin 1 is used.

Sine-wave response at a given frequency depends on amplitude and on which terminal is used for the input. Figure 2 shows the response when the high-impedance input is used. As crest factor* (CF) increases from 1 to 3, up to 0.7% of additional error is produced; with CF of 5 (1-V peak), the additional error is 2.5%, with C_{AV} = C_F = 100 μF. In general, the higher CF, the larger C_{AV} must be to maintain a given level of accuracy.

The table below shows settling times with typical combinations of practical values of C_{AV} and C_F for various input levels and low-frequency cutoffs—and crest-factor ranges—found in a variety of applications.

APPLICATIONS

Figure 3 shows how the AD737 would be applied in a portable 9-volt battery-powered 3 1/2-digit voltmeter, using a 7136-type DPM chip as the a/d converter, which drives an LCD display. High input impedance permits an attenuator to be used for the higher-voltage ranges. The AD737's input is protected by a 47-kΩ series resistor and a pair of 1N4148 diodes, which serve to clamp the input to either end of the supply. Operating on less than 4 milliwatts of power, this circuit will run even if the battery voltage drops to as little as 6 volts.

Input ranging is provided by the standard 10-MΩ input attenuator. AC input coupling is provided by capacitors C and C_1. Because of the a/d converter's high input impedance, the post-filter doesn't require a high value of capacitance; a 1-megohm-0.1-μF R-C filter provides adequate smoothing without loading the 7136's input significantly, while saving board space.

Other applications include wide-range dB-measuring circuits and rms ratio circuits. However, because of the versatility and low cost of these devices, their most popular use will be as a one-chip replacement for average-responding ac measurement circuits, with the bonus of a free upgrade to the kind of ac measurement accuracy only an rms circuit can provide.

The originator of the AD736/AD737 was Lewis Counts, ADI Fellow; the chip was designed by Wyn Palmer; test and trim design were by Andrew Wheeler. All are at Analog Devices Semiconductor, Wilmington MA.

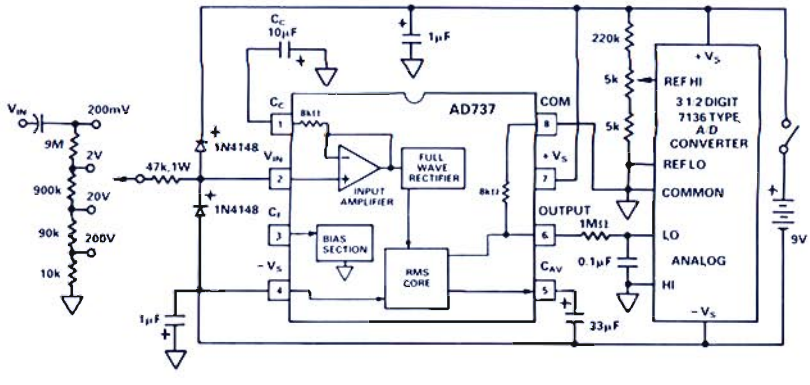


Figure 3. Applying the AD737 in a 3 1/2-digit voltmeter.

*Crest factor for a given input signal is the ratio of peak to rms, a property of the input waveform. Typical crest factors are 1 for square waves, $\sqrt{2}$ for sine waves, and 10 for a square pulse having a 1% duty cycle.

TRUE 18-BIT DAC IN HYBRID PACKAGE HAS SMALL SIZE, LOW COST

AD1139 Is Complete With Latches, Reference, Output Amplifier Includes Range Resistors and Kelvin Connections

by Jeffrey Greenwald and Bill Sheppard

The AD1139 d/a converter (DAC)* provides true 18-bit performance in a hybrid package, smaller and less costly than earlier modular designs. It is *complete* (Figure 1), with all functions —input data latches, precision reference, output amplifier and ranging resistors, and Kelvin connections—needed to translate digital data to voltage that drives a load accurately.

Applications for a DAC of this caliber include automatic test (including equipment for testing ADCs and lesser DACs) and scientific instrumentation (chromatographs, spectrographs), and electron beam positioners. High accuracy and stability mean that calibration of systems using such devices may in many cases not be needed over the product life, a major benefit in the field.

No user adjustments are needed to achieve the specified 18-bit (0.00019%) accuracy, with ±1/2 LSB (±2 ppm) maximum differential and integral nonlinearity (DNL and INL). For a full-scale step (10 V) the DAC's output settles to within 1/2 LSB in 40 μs, and a single-bit change settles in 6 μs; glitch impulse at major carries is 400 mV × 500 ns. INL and DNL temperature coefficients are ±0.5 ppm/°C and ±1 ppm/°C of full-scale range (FSR), and gain drift is a maximum of ±4 ppm/°C, including the reference. The maximum offset tempco is ±1 ppm/°C FSR.

Digital Input Structure: Input to the AD1139 is latched as a single 18-bit 5-V-CMOS-compatible parallel rank. Inputs are binary coded for unipolar output and offset binary for bipolar. A 200-ns *write* pulse latches the data bits; if the *write* line is held active, the latches are transparent to data changes. To interface the DAC input to an 8-bit bus requires only five ICs: two for I/O space address decoding and enabling, and three for latching the data from the 8-bit data bus. Wider buses require fewer ICs.

Analog Output: Pin-programmable internal resistors set the output voltage range to one of four voltage spans: 0 to +5, 0 to +10, ±5, and ±10 V. A current output is available from another pin of the DAC; normally 0 to −1 mA, it can be offset by 0.5 mA via pin strapping to provide a bipolar ±0.5 mA output range.

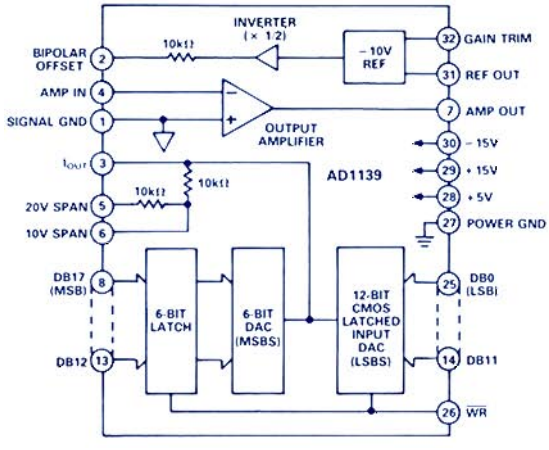
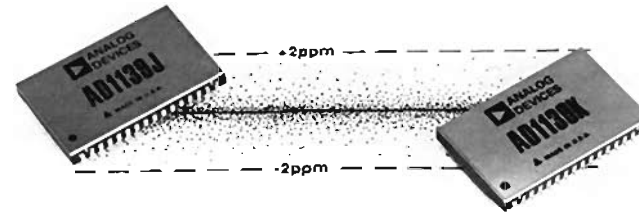


Figure 1. AD1139 block diagram.

*Use the reply card for technical data.



GETTING BEST RESULTS

Offset- and gain-trim pins are provided to reduce initial offset and gain errors. The procedure steps are straightforward—adjust for zero offset, then adjust gain at full-scale output—but at the 18-bit level, great care is necessary. The voltmeter used must resolve to 10 μV for end-point calibration.

Remote Sensing Voltage drops due to line resistance between the output and load can be a major source of gain error and gain temperature coefficents when using a high-resolution DAC. On the ±10 V range, a single bit corresponds to only 76.3 μV (and correspondingly less on the smaller span ranges). A 0.02"-wide copper track, with 50 milliohm/inch track resistance, that connects the output of a DAC to a load just 3 inches away will have a resistance of 0.15 Ω in each direction, a 0.3 Ω total. A 10-mA output current will cause a 3-mV voltage drop, or a 0.03 % gain error (79 LSBs at 18 bits). Variations of the track-resistance effect with temperature cannot be trimmed out (unlike the initial gain error) and can contribute as much as 1.2 ppm/°C to the gain drift.

The AD1139 can be configured to sense the actual output value at the load and feed back a correction; the DAC adjusts its output voltage so as to deliver accurate voltage to the load. When configured as shown in Figure 2, all the load current will flow through the *force* line connected to the internal output amplifier on the high side—and power ground on the low side—of the load, but not through the *sense* lines. The input of the output amplifier senses the load voltage through the DAC feedback resistor; the low side of the load is sensed by the AD1139's measurement ground—where only bias currents flow.

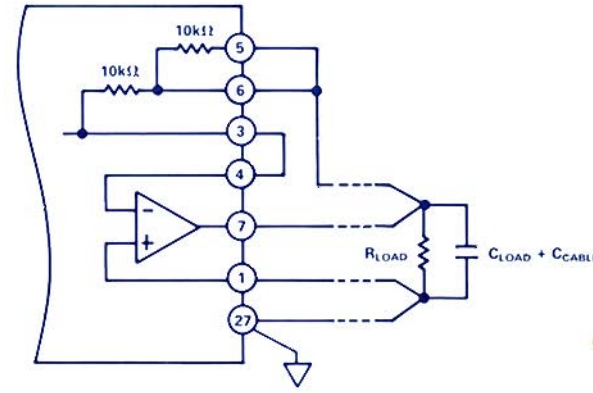


Figure 2. Remote Sensing compensates for lead resistance.

When remote sensing is used, the track-resistance contribution at the remote load is reduced to 0.0015%, with a tempco of less than 0.1 ppm/°C. Although the AD1139's output amplifier can typically drive up to ±20 mA, the load should not exceed ±10 mA or 2,000 pF for rated accuracy and amplifier stability.

Grounding and Ground Currents Because a small amount of current flows through a DAC's signal ground, a length of ground wire or equivalent circuit-board track will cause errors due to voltage drop through the ground lead. Milliohms are critical when one LSB is less than 100 μV, even on the highest range.

This error cannot be calibrated out in most DAC architectures, since the ground current varies with the actual DAC code; this variation produces system nonlinearity and gain errors. A typical range of ground currents is 0 to −2 mA, or ±1 mA. In the AD1139, a combination of techniques makes the ground current independent of the DAC code. The two internal DACs and the voltage reference were initially identified as sources of potential code-dependent ground-current; their design was improved to keep the AD1139 ground current constant, regardless of code.

There are two grounds on the AD1139, the measurement ground and the power ground. The measurement ground is intended to be used for remote sensing to the point considered as the user's high-quality "star" ground. Small bias currents (less than 1 μA) flow from this terminal. The power ground carries analog and CMOS digital supply current from the AD1139, to be returned to the power supply—about 1.5 mA, independent of code.

With separate grounds available, the user can define the system measurement ground instead of having to use the DAC's power ground as a measurement point. This works to advantage in systems with multiple DACS, since the signal grounds can all be connected to a single star point, which in turn can be connected to the digital ground at one point only. For the AD1139 to operate properly, the measurement ground *must* be connected to power ground somewhere in the system, because the two grounds are not directly connected to each other within the DAC. Clamp diodes are used to restrict the open-terminal voltage (*sense* loop open) to a single diode drop from power ground.

The 18 bits of resolution are divided between two DACs within the AD1139. The six most-significant bits are developed by a novel switched-voltage DAC, while the 12 lower-order bits, DB0 through DB11, are converted by 12 bits of a 14-bit current-steering DAC. Its output is converted to a voltage and then back to a current to be properly summed along with the MSBs in the output stage of the AD1139. Typically, R-2R current-steering DACs have nonlinear code-dependent ground current. To eliminate this error source, the DAC ground is driven with a "voltage-follower ground buffer," which provides a convenient sense point to be connected to measurement ground.

Reference: A highly accurate DAC requires a precise, stable reference. The AD1139's −10-volt reference circuit is based on the Analog Devices AD588 IC reference. Initial maximum error of the reference is ±0.1%; temperature compensation results in a maximum tempco of ±3 ppm/°C over the 0 to 70° range. The performance specifications of the AD1139 include reference error. The reference has narrowband noise (0.1 to 10 Hz) of 10 μV peak to peak (p-p) and wideband (100 kHz) noise <50 μV rms.

A buffered version of the reference is available for external applications, such as ratiometric device testing. When the AD1139's REF OUT is used as the reference for a DAC under test, Figure 3, the gain of the DUT will track the AD1139 gain; the reference's contribution to gain error is thus eliminated.

As a reference DAC for testing linearity, the AD1139 measures to 1/32 LSB of uncertainty for 14-bit DACs, 1/8 LSB for 16-bit devices. The integral-linearity error is the difference between the outputs of a reference AD1139 and the DAC under test. For differential linearity error, the DAC digital input is stepped and the new output is compared with the previous output—any difference from the ideal is a differential linearity error.

External Output Amplifier: The AD1139's output amplifier is optimized for very low noise, dc-stable applications and moderate settling time. For higher speed or more output current, an external op amp is used instead of the internal amplifier (Figure 4). The AD711 is a good choice for higher-speed applications; it will settle to within 16 bits in only 6 μs for a unipolar full-scale step. Other amplifiers may be chosen for differing tradeoffs. The noise gain, as seen by the output amplifier, depends on the output voltage range selected: it is 2 for 0 to +5 V range, 3 for 0 to +10 V, and 7 for the ±10 V range. The amplifier selected must be stable at the noise gain corresponding to the output range.

Two grades of the AD1139 are available; the ±1-LSB J and the ±1/2-LSB K are both packaged in a hermetic 32-lead triple-width DIP package. Prices (100s) are $195 and $295.

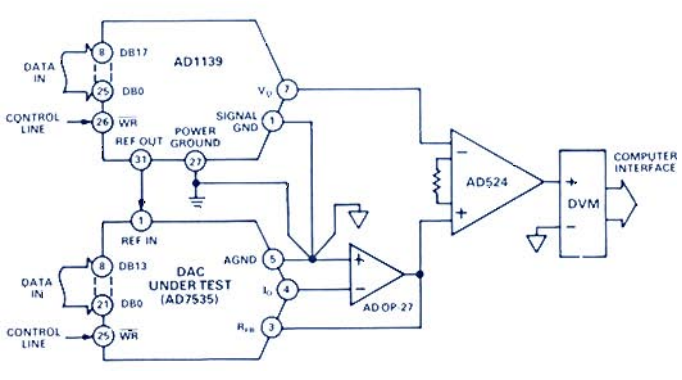


Figure 3. Ratiometric testing of 14- and 16-bit DACs with the AD1139.

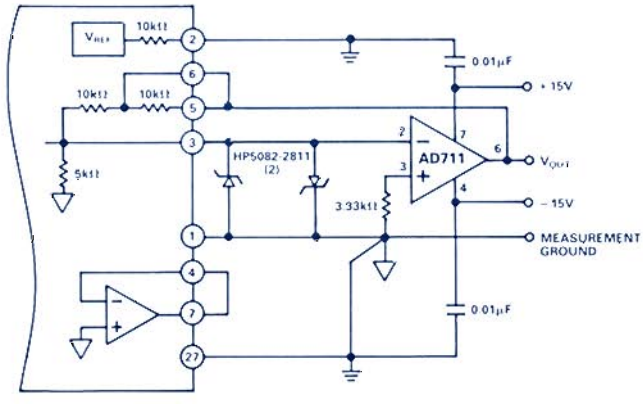


Figure 4. External amplifier for augmented DAC-output performance.

12-BIT ADCs FOR DSP PROVIDE COMPLETE INTERFACE

Single-Channel AD1332 Has S/H, Filter, FIFO, Digital Interface

Multichannel AD1334 Can Do Simultaneous Sampling

by Bob Malone and Rene Sierra

The AD1332 and AD1334 sampling a/d converters,* with 12-bit resolution and accuracy, provide the functions necessary for a complete interface between audio-bandwidth signals and digital signal-processing systems. The 40-pin-DIP-packaged hybrid devices provide a space-saving, system-level means of data acquisition for DSP applications, replacing a board-full of ICs.

The *single channel AD1332* combines a sample/hold amplifier with an anti-aliasing filter and 12-bit A/D converter; the *AD1334 converter provides 4 input channels* which can used independently or sampled simultaneously. The digital side of these converters is fully asynchronous, with extremely fast (15-ns) bus-access time; included is a 32-word first-in first out (FIFO) memory to make the interface between the converter and the processor transparent and efficient. Because the AD1332 and AD1334 convert asynchronously; there is no need to synchronize the sampling clock and the system clock.

This digital interface design greatly simplifies the circuitry and software needed to transfer digitized signals to the processor. High-speed DSP processors, such as the ADSP-2100/2100A (see page 20), TMS320C25, and DSP56000, can access data directly without an inefficient "wait state." The 32-word FIFO decouples the data sampling and conversion cycle from the needs of the processor and its software timing; conversion results can be transferred as a group to the processor memory, rather than singly.

AD1332 SINGLE-CHANNEL FRONT END

A block diagram of the AD1332 is shown in Figure 1. The converter is scaled for a ±5 V input signal range, using an internal precision reference. The sample/hold operates on a band-limited input signal prior to conversion by the ADC. S/H and conversion timing are set by an externally applied 20 × clock; a clock frequency of 2.5 MHz will achieve the maximum sampling rate of 125 kHz. The clock must be stable, since clock jitter affects the precision of the sampling period.

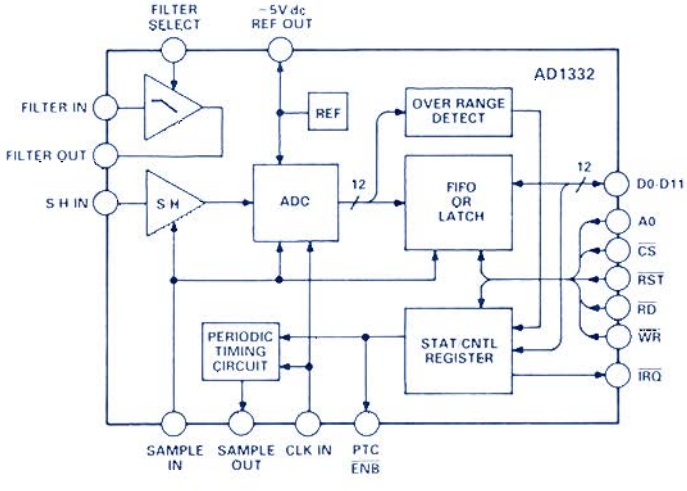
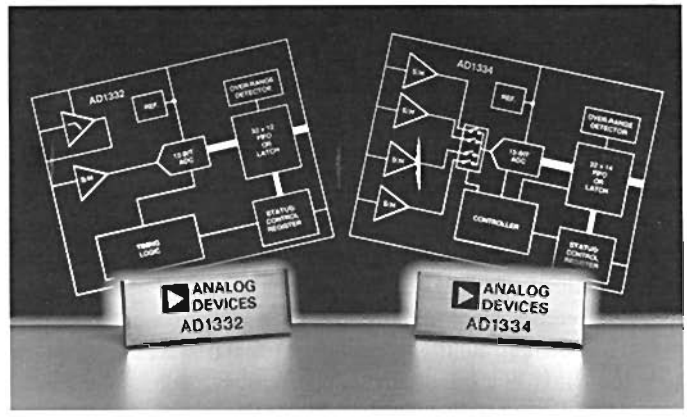


Figure 1. AD1332 block diagram.

*Use the reply card for technical data.



Two conversion modes are available. In the *periodic* timing mode, sampling and conversion proceed continuously, at the rate determined by the clock—useful where data will be processed continuously, as in digital filters or FFTs. The other mode is *externally triggered* conversion, where sampling and conversion take place only after the *Convert Start* control line goes active. This mode's maximum conversion rate is 110 kHz unless the trigger is synchronized to the clock.

The AD1332's internal anti-aliasing filter is intended to limit bandwidth. Sampling theory states that a signal can be fully represented and reconstructed from $2N$ samples per second for a signal that is bandwidth-limited to N Hz. Sampling at $<2N$, or sampling signals with bandwidths $>N$, results in aliasing, which makes it impossible to reconstruct the original analog signal. That's why the input-signal bandwidth must be limited.

The AD1332's filter is an active 4-pole Butterworth low-pass. The user can set the cutoff frequency, f_c, at up to 50 kHz with four identical capacitances. The Butterworth filter was chosen because it provides maximally flat magnitude response in the passband. Attenuation at the cutoff frequency is 3 dB, and rolloff beyond f_c, 20 dB/decade per pole, totals 80 dB/decade. Figure 2 shows passband and stop band responses for f_c of 25 kHz and 50 kHz. Guaranteed minimum attenuation is 45 dB at $4f_c$ and 76 dB at $10f_c$.

The filter uses low-noise, high-speed op amps for low distortion and consistent frequency response over the entire range. Precisely trimmed thin-film resistors give consistent and accurate filter setting with user-supplied capacitors. Unlike switched-capacitor filters (which are sampled-data systems), the filter in the AD1332 does not require a clock, pre-filtering, or post-filtering. Although present, the filter is optional. *External* filters allow connection of the input signal directly to the S/H input, or a programmable-gain amplifier between the filter and the ADC.

To meet the needs of DSP applications, the device is specified for both static (dc) and dynamic (ac) performance. Integral nonlinearity over temperature is ±1/2 LSB typical, ±1 LSB maximum. The full-scale error is ±2 LSB at 25° C, for both + and − FS.

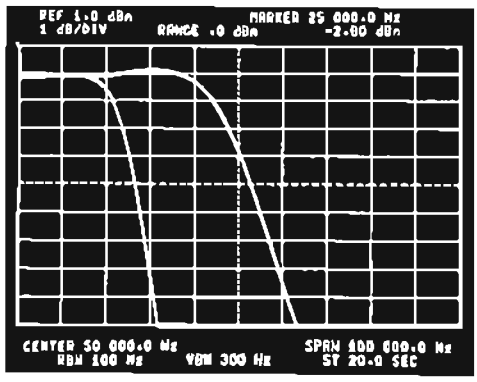
Dynamic specifications: with the anti-aliasing filter set to f_c of 50 kHz and an input sine wave of 38.7 kHz, signal-to-noise ratio (SNR) is 70 dB, corresponding to 11.3 effective bits. Total harmonic distortion (THD)—same input conditions—is at least 72 dB below the fundamental (Figure 3). Intermodulation distortion (IMD) with inputs of 32.8 kHz and 34.3 kHz is also at least 72 dB down. Results are similar without a filter and 60-kHz input.

AD1334 FOUR-CHANNEL FRONT END

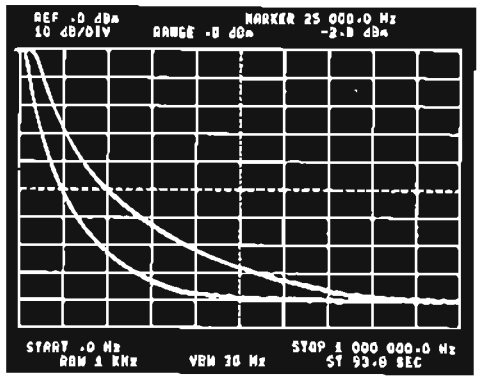
Each input channel of the AD1334 has its own S/H, which provides signals to the high-speed 12-bit ADC via the multiplexer (Figure 4). Anti-alias filtering is user-provided externally. The channels can be digitally programmed to operate either independently or in concert. All four channels can be sampled simultaneously (and converted sequentially) at rates up to 28 kHz; the maximum one-channel-only sampling rate is 65 kHz. The four channels can be sampled at differing rates.

The low effective S/H aperture-delay-time mismatch and aperture uncertainty from channel to channel and device to device are essential where the signal phase information and relationships are as important as amplitude, e.g., in phased-array sonar, medical ultrasound, and multiple-axis position control.

Integral and differential nonlinearity are typically less than ±1/2 LSB (±1 LSB over temperature). Full scale error is ±2 LSB maximum at 25° C and typically half as much. Total harmonic distortion and intermodulation distortion are 72 dB below the fundamental; the 70-dB SNR corresponds to 11.3 effective bits, very close to the theoretical maximum of 12 bits.



a. Passband response. Scale: 10 dB/div, 10 kHz/div.



b. Stopband attenuation. Scale: 10 dB/div, 100 kHz/div.

Figure 2. AD1332 filter responses at 25 and 50 kHz.

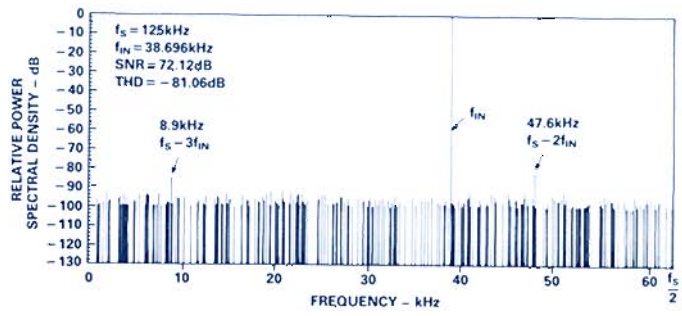


Figure 3. AD1332 spectral response, with filter; note low level of aliased harmonics.

DIGITAL INTERFACE

Both devices have 32-word FIFO memories. The FIFO in the single-channel AD1332 is 12 bits wide, but the AD1334's FIFO is 14 bits wide, to store both the 12 bit conversion data and a 2-bit channel identification code. Interrupts indicate to the processor that data is available.

Interaction between the converters and the processor is managed by a *control* byte and a *status* byte. The *control* byte sets FIFO operating mode and sampling conversion mode (periodic or triggered). The *status* byte indicates FIFO conditions; it can either be polled by the processor or read after an interrupt.

The control word sets the interrupt to occur when the FIFO is full, half-full, or indicating analog overrange (beyond the ±5 V range). This last setting allows the analog range to be changed immediately to prevent useless conversions from continuing. There is also a *transparent* mode, effectively bypassing the FIFO, where the result of each conversion is available immediately without waiting for it to propagate through the FIFO. Upon the interrupt, the processor can quickly access all results in the FIFO in a single burst, even while another conversion is occurring.

The interface between a DSP processor and the AD1332 or AD1334 usually requires only a simple address decoder. The fast data access—15 ns—results in zero wait states; no special wait state circuitry or handshake lines are needed for DSP ICs available today and known members of the next generation. Internal three-state buffers connect directly to the processor bus.

Both the AD1332 and the AD1334 operate from ±12 to ±15 V supplies. Total power consumption is <2 W, maximum, and operation is specified for the −40° to +85° C temperature range. Devices will be available screened to MIL-STD-883B. Prices begin at $140 (100s) for the AD1332 and $180 for the AD1334.

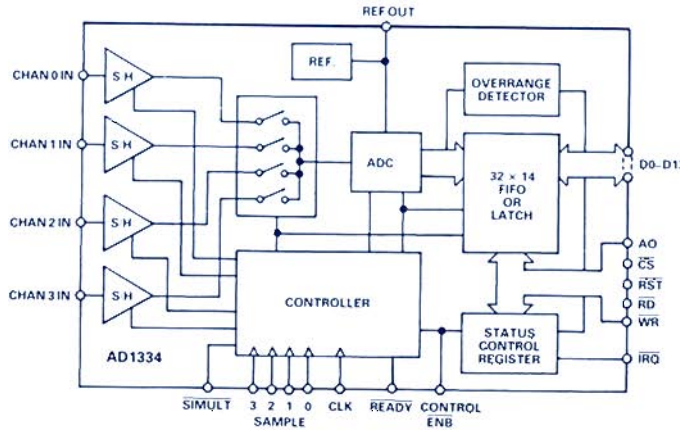


Figure 4. AD1334 block diagram.

MONOLITHIC DIGITALLY PROGRAMMABLE DELAY GENERATOR

AD9500 Converts an 8-Bit Digital Input to an Output Time Interval FS Range Is from 2.5 ns (with 10-ps Resolution) to 100 μs And More

The AD9500 Programmable Delay Generator* receives a digital *trigger* pulse and outputs a signal after a specified delay period, as programmed by an 8-bit digital input. The full-scale delay range is flexible, ranging from a few nanoseconds to more than 100 μs; it is set by an externally connected R-C combination. Compact, low-cost single-chip digitally programmable delays have immediate practical applications in test systems: eliminating signal skews in high-speed systems, measuring unknown delays, and constructing programmable ring oscillators.

Figure 1 shows the various functions within the AD9500. The key functions are the reference and the timing-control circuit—which form an analog integrator; an 8-bit d/a converter, set by the 8-bit digital control input; and a high-speed precision comparator with complementary ECL outputs. Inputs are differential *trigger* and *reset* signals, which may also be used with single-ended inputs. The maximum triggering rate is 100 MHz.

HOW IT WORKS

The *trigger* and *reset* inputs are designed primarily for ECL signal levels, but they can function with analog and TTL input levels. An on-board reference midpoint allows both of the inputs to be driven by either single-ended or differential ECL circuits.

As the timing diagram in Figure 2 shows, the delay is initiated when the trigger input goes *high*. The integrator generates a downgoing ramp; when it crosses a level established by the 8-bit DAC, the comparator output changes state, producing the delayed outputs, Q and $\overline{Q}$. A parallel $\overline{Q_R}$ output circuit is available for uses where the AD9500 drives its own *reset*.

Its delay is equal to the programmed delay, t_D—a function of the selectable RC time constant (Figure 3) and the precision threshold set by the DAC—plus a propagation delay (t_{PD} = 7.4 ns max with a 5-ns full-scale input).

$$\text{Total delay} = t_{PD} + t_D$$

$$= t_{PD} + \frac{\text{digital value}}{256} R_{SET} (C_{EXT} + 10\text{ pF})$$

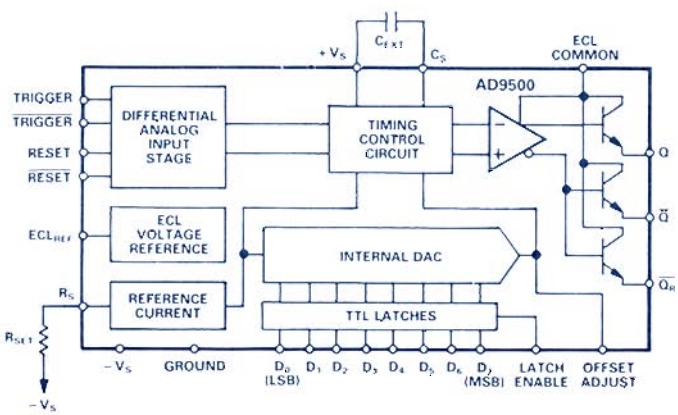
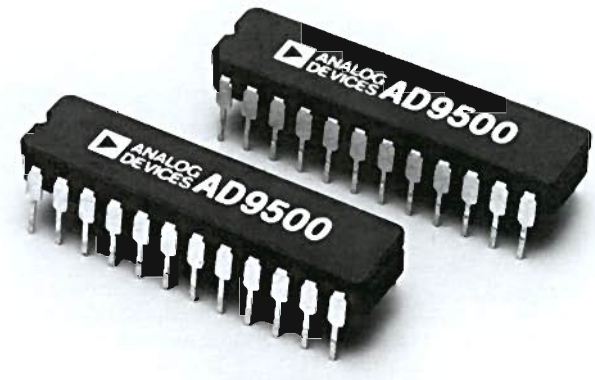


Figure 1. Block diagram of the AD9500.

*Use the reply card for technical data.



Reset: A pulse of appropriate width applied at the Reset input resets the integrator and the Q outputs to prepare the device for the next trigger. At the end of the reset propagation delay (t_{RD}, approximately equal to t_{PD}), Q returns to its original state; 0.2 ns after the Reset input goes low, the device is ready for the next trigger. A *reset* interval, t_{LRS}, should be allowed for the linear ramp to return and settle to its original level.

When C_{EXT} = 0, and R_{SET} = 250 Ω, the full-scale programmed delay time is 2.5 ns, and the LSB (one increment of delay) is 2,500 ps/256 ≈ 10 ps, which is also the typical jitter level; this establishes the basic delay-time resolution.

The digital control data is passed to the AD9500 via a transparent latch, controlled by the *latch enable* signal. In the transparent mode, the DAC follows changes at the inputs; the *latch enable* signal is used to strobe the digital data into the AD9500's latches.

Because the DAC has fast response, the programmed delay may in principle be updated in the same time frame as the signals being

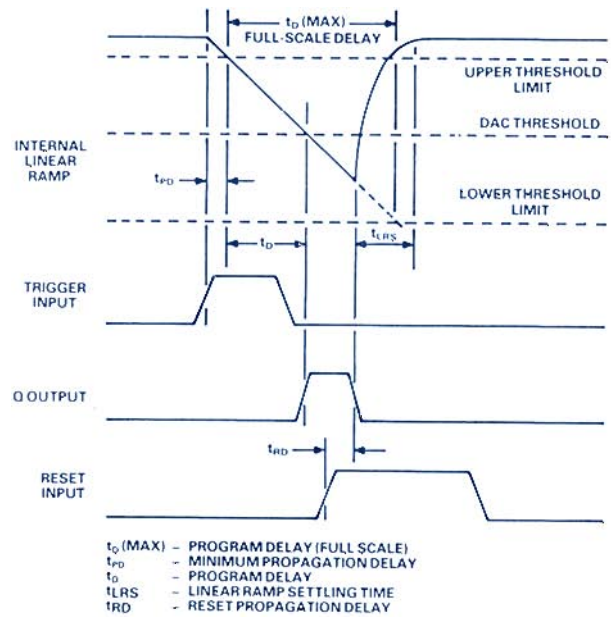


Figure 2. Timing diagram.

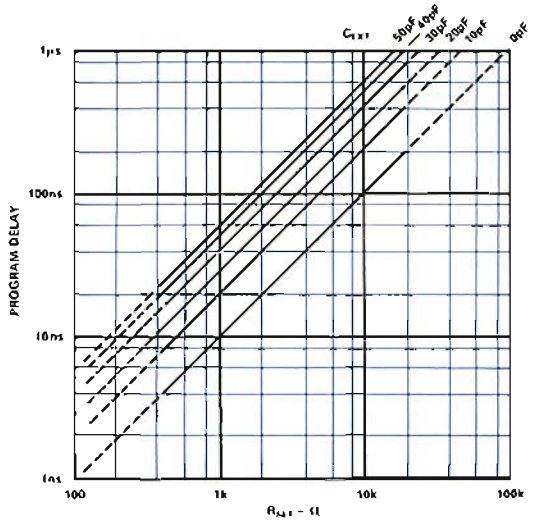


Figure 3. Typical values of programmed delay ranges as a function of resistance and capacitance.

delayed. However, the next trigger should wait for the DAC to settle, typically 29 ns after latching in a new value.

The AD9500's programmed time delay is linear to within 1 LSB maximum integral nonlinearity with >100-ns full-scale input, with 1/2-LSB max differential nonlinearity; monotonicity is guaranteed over the full specified operating temperature range. 312mW of power is drawn from the +5-V and −5.2-V supplies.

Devices are graded to operate from −25 to +85°C (B grades) and −55 to +125°C (T grades). Except for operating temperature range, all grades have identical electrical specs. Available packages include 28-pin PLCC (P) and LCC (E) packages and 24-pin ceramic "skinny" DIPs (Q). Prices in 100s start at $16.00.

APPLICATIONS

Multichannel Deskewing: A highly effective use of the AD9500 is in multiple delay-matching applications. For example, in a high-speed, high-pin-count logic tester, slight differences in impedance and cable length can create large timing skews. The high speed of modern test systems makes timing accuracy particularly important, and the large number of driver lines (e.g., 128 driver lines with switching capabilities in excess of 100 MHz) requires the use of compensating circuitry. In practice, each signal line would drive an AD9500; its output would drive a logic test-head line (Figure 4). With one line as a standard, the programmed delays of the others are adjusted to eliminate the timing skews.

With the very fine timing adjustments possible from the AD9500 (as small as 10 ps), nearly any high-speed system should be able to adjust itself automatically to within very tight tolerances.

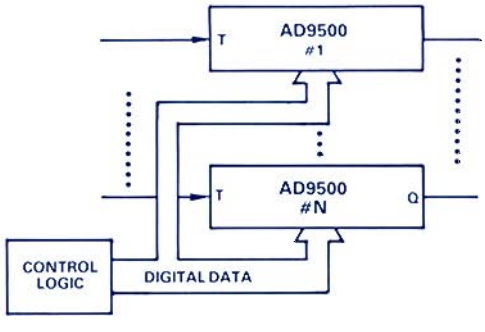


Figure 4. Multiple delay matching.

Measuring Unknown Delays: Two AD9500s can measure delays precisely (Figure 5). One is set with little or no programmed delay; its output drives the unknown-delay circuit, which in turn drives the input of the "D"-type flip-flop. The second AD9500 drives the *clock* input of the flip-flop. With both triggered together repetitively, the programmed delay of the second unit is varied to detect the output edge from the unknown delay.

Detecting the output edge is straightforward. If the programmed delay through the second AD9500 is too long, the flip-flop output will be at logic *high*—if too short, at logic *low*. When the unknown is very closely matched, the flip-flop's output will bounce between *high* and *low*. The digital code value used to create the second programmed delay is a direct indication of the delay though the unknown circuit. Best results are achieved by calibrating the system with the unknown delay removed.

Programmable Oscillator: A digitally programmed oscillator for frequencies up to 67 MHz is an interesting use of the AD9500. The high-precision delays it generates can be exploited to create a ring oscillator with variable duty cycle (Figure 6). The delayed output of the first AD9500 is used to drive the *trigger* input of the second unit; the output of the second, in turn, drives the *trigger* input of the first. Together, the devices will alternately trigger one another, creating two pulse chains on their outputs.

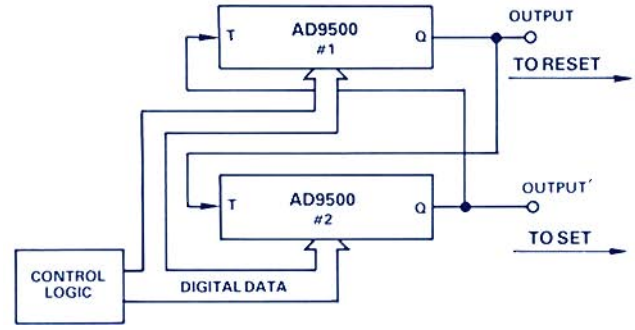


Figure 5. Programmable oscillator.

The total delay through both AD9500s determines the period of the oscillation. The duty cycle can be controlled by using the outputs to drive the *set* and *reset* inputs of a flip-flop. The delay through the first AD9500 controls the flip-flop logic *low* output pulsewidth; the second controls the logic *high* pulsewidth.

The AD9500 was designed by Jeff Barrow at ADI's Computer Labs Division, in Greensboro NC. Critical portions of this circuit are covered by U.S. Patents 4,742,331 (Jeff Barrow and A. Paul Brokaw) and 4,349,811 (A. Paul Brokaw). ◘

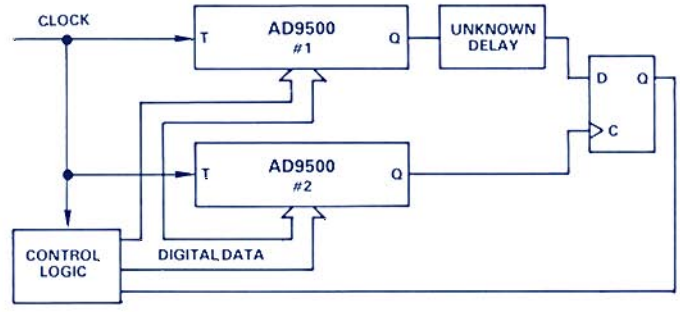


Figure 6. Measuring unknown delays.

15 NEW CMOS SWITCHES AND MUXES IN CONVENIENT VARIETY

ADG Series Is Spec'd for 44-V max Supply, Wide Temperature Range, Single-Supply

Superior 2nd Sources Include ADG-201HS: 50-ns t_{ON}

Fifteen additions to Analog Devices' line of CMOS switches and multiplexers (muxes) give designers a choice of components optimized for the application. The ADG201A/202A* (utility), ADG201HS (high-speed)*, ADG211A/212A* (lowest cost), and ADG221/222 (latched) quad switches—and the multiplexers in the ADG506A/507A & 526A/527A (16/dual-8-channel),* and the ADG508/509A & 528A/529A* (8/dual-4-channel) families—are specified for dual- and single supplies and for applications with higher supply voltages and wider temperature ranges than many of the industry-standard namesakes that they replace.

Avoiding dielectric isolation, these components are fabricated at low cost in a high-performance, linear-compatible CMOS process (LC^2MOS) with a breakdown voltage of 44 V. The normal operating voltage range is ±10.8 to ±16.5 V, but the devices can operate with supply voltages up to the breakdown voltage. Low leakage currents (≤1 nA at 25° C) minimize offsets.

The self-aligned high-voltage switch process results in much lower parasitic capacitances than dielectric isolation, with correspondingly higher switching speeds. The basic switch is latchup-free over the full operating range; advanced design and process techniques eliminate latchup-prone parasitic transistors.

ANALOG SWITCHES

The ADG201A & 201HS, ADG202A, 211A, 212A, 221, and 222 are quad SPST switches; each switch is independent of the other three in the package (Figure 1). The xx1's and xx2's differ only in the sense of their control logic, as shown in the table. The digital control signal can be either TTL or 5-V CMOS compatible. The latches in ADG221/222 permit switch-state storage.

A low charge-injection design minimizes transients that occur during switching. All switches are "break before make," an advantage in multiplexer applications, since the outputs of the switches can be safely tied together. The analog signal range that can be handled is ±15 V. The switches can be operated from a single +15-volt supply for unipolar (0 to +15-V) analog signals.

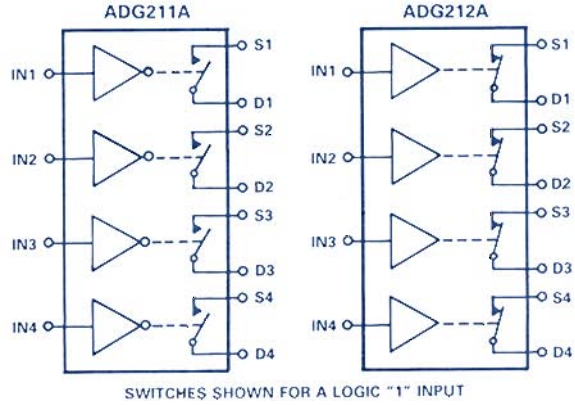
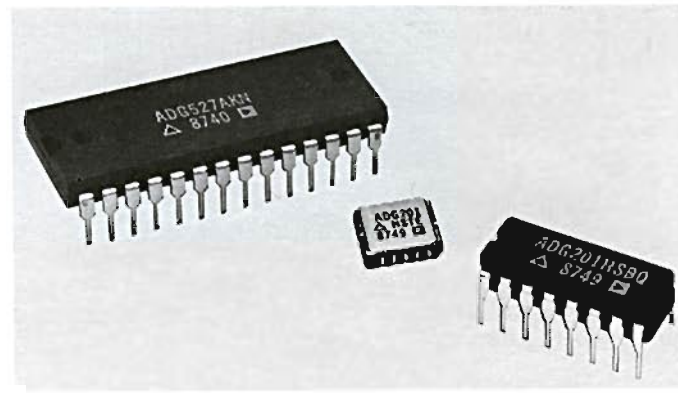


Figure 1. Block diagram of complementary quad switches.

*Use the reply card for complete data sheets on any of these product pairs and to request the short-form guide: *Analog Switches and Multiplexers*.



COMPARING ADG QUAD SWITCHES

ADG:	201A/ 202A	201HS	211A/ 212A	221/ 222
Logic for OPEN	1/0	1	1/0	1/0
Latches	No	No	No	Yes
R_{ON} max (25°C)	90Ω	50Ω	115	90Ω
R_{ON} max (T_H)	145Ω	75Ω	175Ω	145Ω
Turn-on Time,25°C,max	300 ns	75 ns/50 ns	600 ns	300 ns
Turn-off Time,25°C,max	250 ns	75 ns/50 ns	450 ns	250 ns
Grades (Temp. Ranges)	K,B,T[1]	J,A,S/K,B,T[2]	K[1]	K, B, T[1]
Packages[3]	N, Q, E	N, Q, E, P	N, P	N,Q
Lowest-Price Unit(100s)	$3.15/$2.95	$3.10/$4.80	$1.60	$2.56

[1]Temp. Ranges: J, K = 0°C to 70°C, A, B = −25°C to +85°C, S,T = −55°C to +125°C.
[2]Temp. Ranges: J, K = −40°C to +85°C, A, B = −40°C to +85°C, S, T = −55°C to +125°C.
[3]Packages: N=Plastic DIP, Q=Cerdip, E=LCC, P=PLCC.

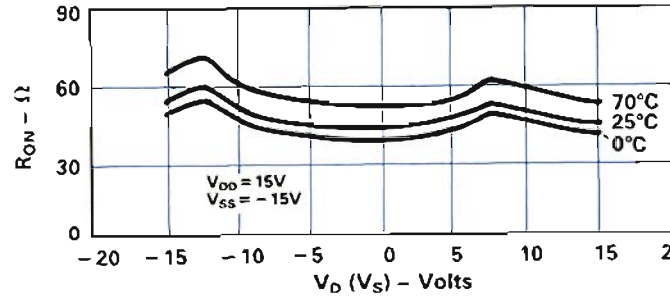


Figure 2. R_{ON} versus temperature for ± 15 V supplies.

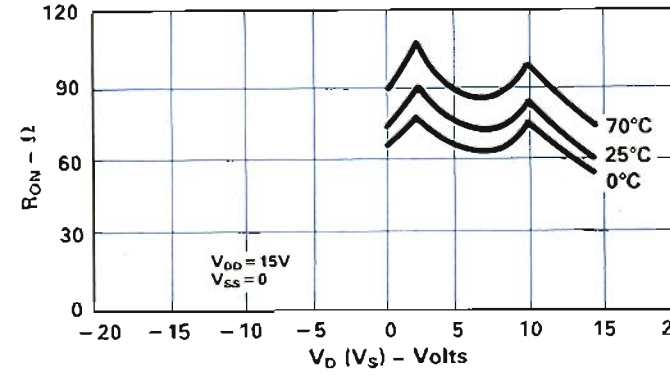


Figure 3. R_{ON} versus temperature for single + 15 V supply.

An important specification that affects accuracy of the final system design is the *on* resistance, R_{ON}; its maximum values at both +25°C and T_H are shown in the table. Note that, for both single and dual supplies (Figures 2 and 3), the *on* resistance does not vary by more than 2:1 over temperature. Switch turn-on and turn-off times are also critical; they too are shown in the table. Data sheets* show characteristics for both dual- and single-supply operation. Power consumption of these switches is less than 33 mW, except for the ADG201HS (240 mW max).

ANALOG MULTIPLEXERS

Multiplexers select one of *N* analog signals and direct the selected signal to a single line. Since the signal flow for analog muxes is bidirectional, they can also be used as demultiplexers to direct a single input to one of *N* outputs. Muxes enhance the basic analog switch by providing address decoding; some devices also have internal latches to facilitate interfacing with microprocessor busses. These recent additions to the ADG family provide designers with a choice of basic features:

MULTIPLEXERS

	Single or Dual	No. Channels	Latches?
ADG506A	Single	16	No
ADG507A	Dual	8, 8	No
ADG526A	Single	16	Yes
ADG527A	Dual	8, 8	Yes
ADG508A	Single	8	No
ADG509A	Dual	4, 4	No
ADG528A	Single	8	Yes
ADG529A	Dual	4, 4	Yes

Single-channel devices switch a single line, while the dual devices switch two lines simultaneously. Thus the single-channel devices can switch analog signals that share a common ground, while the dual devices can switch differential signals; they can also be used to switch two unrelated single-ended signals at the same time.

The desired mux channel (Figure 4) is selected via TTL-and-5-V-CMOS-compatible parallel address lines with binary-coded channel-control signals, decoded within the mux. In non-latched devices, the *enable* input operates the switches when the address bits are valid; when the *enable* line is *low*, all switches within the mux are *off*, with no memory of the last address.

Latched address encoders are used in system designs where the address information must be retained after an address is presented and removed. A processor bus can present this address as data during a *write* cycle, then continue with unrelated data. Latched muxes greatly simplify connection to a bus. Two control lines, *enable* and *write*, make the mux look like a writeable memory location. Address bits are written when the *enable* line is high and the *write* line is low; when *write* goes high, the address is latched and held until purposely overwritten. The *write* pulse must be 100 ns wide, compatible with the timing of most processor busses.

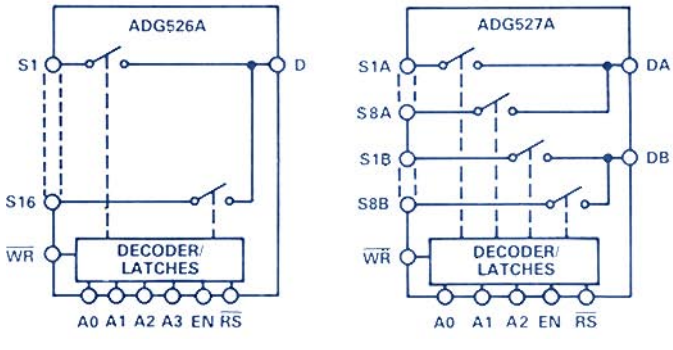


Figure 4. Latched 16- and dual 8-channel multiplexers.

A third control line, *reset*, when *low* clears both the address and *enable* data and forces all switches *off*, resulting in no output. This line is normally connected to the microprocessor *reset* line to insure that the mux has a known, benign state on power up. If reset is not needed, the *reset* line can be permanently set *high*.

Leakage of the mux devices when *off* is only 1 nA max at 25°C (with ±10V supplies). Figure 5 shows the typical leakage as a function of temperature using power supplies of ±16.5 V. Leakage current decreases with supply voltage.

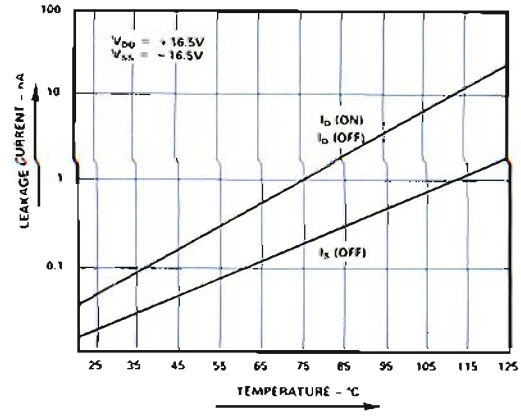


Figure 5. Leakage current versus temperature.

The switching time of the mux, known as *transition time*, characterizes the dynamic performance when switching from one address to another. The transition time for these muxes is 300 ns max at +25°C (400 ns max over temperature) for dual supplies; comparable figures are 450 ns max and 600 ns max for single-supply operation. Transition time decreases with increased supply voltage. Figure 6 shows the typical variation in $t_{transition}$ with supply voltage for the ADG508A and ADG509A.

The muxes are specified for operation over: −40° to +85° C (K & B grades) and −55° to +125° C (T grades). Power consumption is less than 28 mW over the full temperature range. They are available in plastic DIP (KN), plastic leaded chip carrier (KP), hermetic DIP (BQ and TQ), and leadless ceramic chip carrier (TE), and can be qualified to MIL-STD-883B. Prices vary with model, from $3.95 to $7.75 for plastic DIPs (100s).

These CMOS switching devices were designed by Colin Price (now at Analog Devices, Newbury, U.K.) and Tim Cummins at Analog Devices BV in Limerick, Ireland.

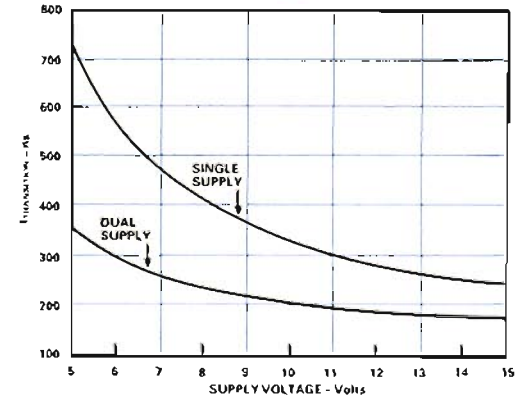


Figure 6. Transition time versus supply voltage.

FAST MONOLITHIC LOG AMP WITH BETTER THAN 250-MHz BW

AD9521 Approaches Performance of Expensive Hybrid Designs

Use It for Successive-Detection RF Strips

by Tom Tice

The AD9521* is a monolithic wideband ac logarithmic amplifier with typical gain of 12 dB. Wideband log amplifiers are cascaded to form "strips" with gains of 90 dB and more, for frequencies typically in the range of 7MHz to 250 MHz. The AD9521, a superior replacement for the monolithic SL521, has performance nearly comparable to the hybrid SL1521.

Amplifiers in the class of the AD9521 are essentially *limiting amplifiers*, providing high gain for small signals and low gain for large signals. They accept high-frequency ac signals (7 MHz to 250 MHz) and provide two outputs (Figure 1): a linear, but saturating, radio-frequency output (voltage) and a logarithmically detected output (current). The detected-output characteristic (current output vs. rf input) on a semilog scale is S-shaped, starting with zero slope, increasing to linear, then soft-saturating.

They are used in *strips*, or cascades, of n (for example, 6 to 9) stages, with the r-f output of one unit becoming the input of the next, thus multiplying their gains (Figure 2). The nonlinearly detected (or *video*) outputs are connected together for current summation.

The resulting output-vs.-input characteristic (semilog scale) is S-shaped, with a lengthy log-linear region whose extent depends on the number of stages (typical gain of 12 dB per device). Once an amplifier saturates, its contribution to the summation is fixed; thus the maximum output for large signals is n times the full-scale output of one device. The maximum dynamic range is realized when the number of stages, n, is the smallest number that causes the input-stage noise alone to produce full output at the last stage.

HOW IT WORKS

Figure 3a shows a typical plot of r-f output voltage vs. r-f input voltage for a representative device. The voltage gain in the linear

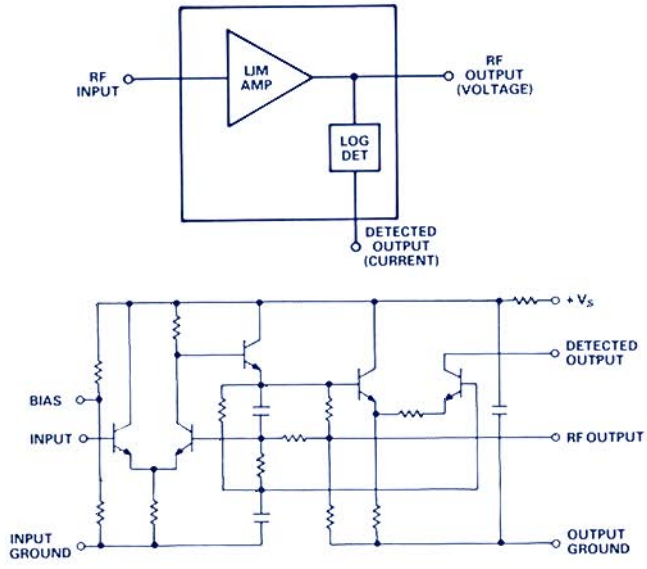
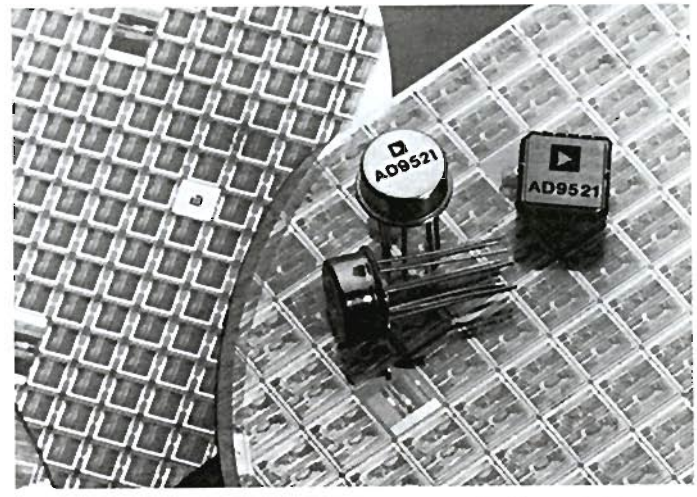


Figure 1. Block diagram and simplified schematic of the AD9521.

*Use the reply card for technical data.



region (to about 100 mV) is 4, or about 12 dB. Beyond 100 mV, the amplifier saturates at about 460 mV.

Figure 3b shows a plot of detected output current vs. r-f input voltage (on a logarithmic scale). The output is seen to range from a floor of 30 μA for low-level signals to a saturated maximum of 1.05 mA, with a log-linear region from about 25 mV to 100 mV (corresponding to output of about 200 to 930 μA). These numbers can of course differ somewhat from unit to unit.

When stages are cascaded, the rf input to a given stage is amplified by 4 to become the r-f input to the following stage. Thus, for a given value of input to a cascade of four units, say 5 millivolts, the output of the first stage (and input to the next) is 20 mV, the input to the third is 80 mV, the input to the fourth is 320 mV, and the output of the fourth (in saturation) is 460 mV.

The corresponding output *currents*, according to Figure 3b, are 30 μA, 120 μA, 820 μA, and 1,080 μA, for a total of 2.05 mA. The table below, illustrating the results for inputs of 1.67 mV, 5 mV, and 15 mV (in equal ratios of 3:1), demonstrates the logarithmic behavior of the cascade; equal input ratios of 3:1 produce total output currents with equal differences of 810 μA.

Stage	Stage Input	Detector Output	Stage Input	Detector Output	Stage Input	Detector Output
1	1.67 mV	30 μA	5 mV	30 μA	15 mV	60 μA
2	6.67 mV	30 μA	20 mV	120 μA	60 mV	660 μA
3	26.7 mV	230 μA	80 mV	820 μA	240 mV	1,070 μA
4	107 mV	950 μA	320 mV	1,080 μA	460 mV	1,070 μA
Total Det. Output		1,240 μA		2,050 μA		2,860 μA
Difference			810 μA		810 μA	

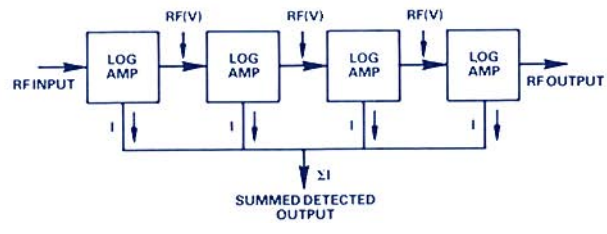
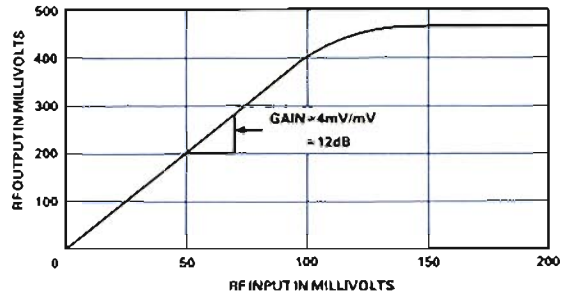
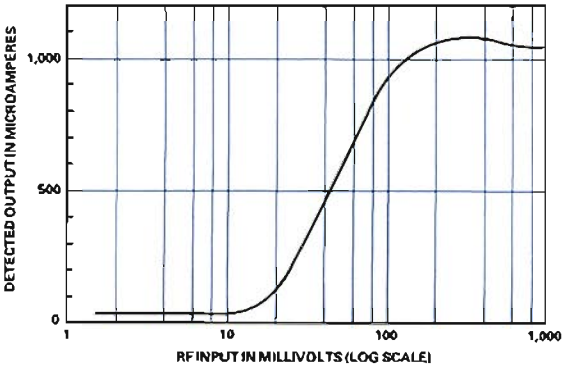


Figure 2. Using log amplifiers in successive detection.



a. R-F output vs. input (linear scale).



b. Video output vs. input (log scale).

Figure 3. Typical log amp output/input characteristic.

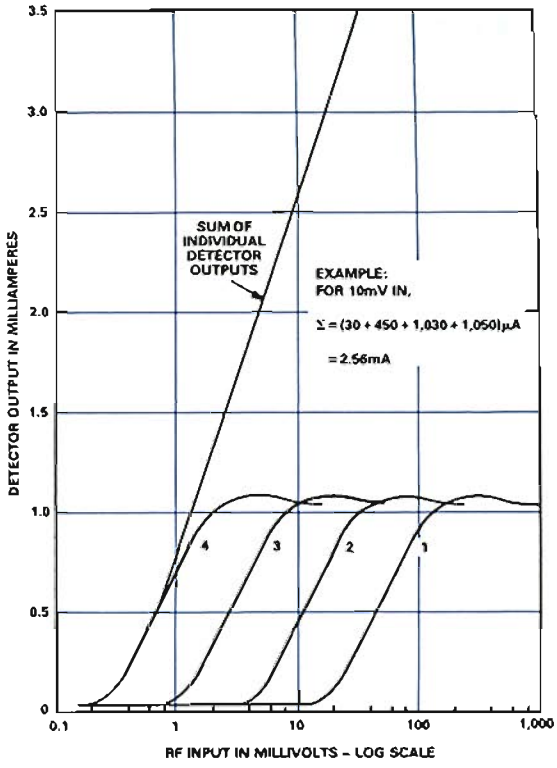


Figure 4. Example of combined response of four log amps.

This relationship is summarized graphically in Figure 4. The current-out vs. voltage-in (semilog) plots for all four stages are combined on a single plot, each displaced horizontally by its per-stage gain of 4. Thus, for a given value of input, the outputs of all stages line up vertically. The sum of these four outputs, when plotted, is a straight line except for the initial curvature below 1 mV and saturation beyond 100 mV: 40 dB of linearity.

Since each stage has a gain of 12 dB, the *maximum* gain is 48 dB. As more sections are added, additional S-curves appear on the plot to show the increase in total gain and dynamic range, increasing the log-linear total to include ever-smaller inputs, until the noise threshold is reached. Figure 5 is an example of a typical log strip. The AD9521 can be used in log strips with gain up to 90 dB.

PERFORMANCE

Guaranteed minimum gain at any temperature and at frequencies from 30 MHz to 160 MHz for any device grade is 11 to 11.7 dB, depending on frequency, with typical gains ranging from 12.2 dB to 13.4 dB, increasing with frequency. Typical upper cutoff frequency is 245 MHz, with lower cutoff at 7 MHz; min-max specs over temperature are 200 MHz and 10 MHz. Typical propagation delay is 1.4 ns. Current drain at +6.0-V supply is 16.5 mA max over temperature, with 84-mW typical dissipation.

Devices are available for 0°-70°C (J/K) and −55°C to +125°C (S/T); Hermetic cans (H package) are available for *all* grades, with LCCs (E) available for S/T grades. K/T grades have tighter tolerances on guaranteed current output than J/S, depending on frequency and temperature range. Prices start at $16 (100s).

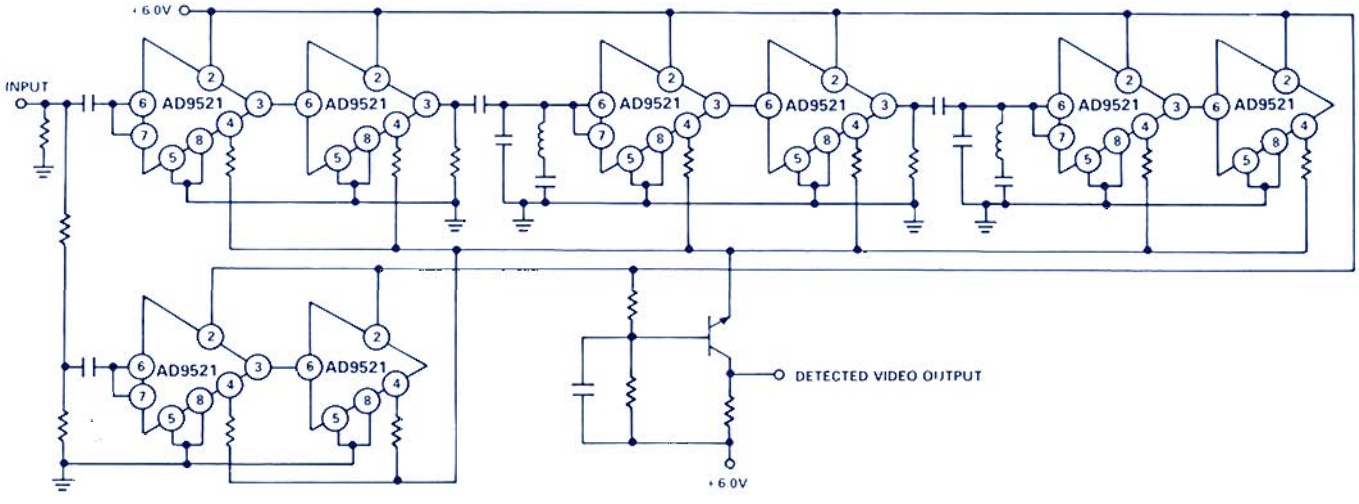


Figure 5. Typical AD9521 log-amp strip configuration.

FASTER DSP μP: 1,024-POINT RADIX-4 FFT IN 3.0 ms

ADSP-2100AK Runs at 12.5 MHz; Available in 100-Lead PGA or PQFP
Evaluation Board, ANSI C Compilers, Other Cross-Software Available

The ADSP-2100A* is a faster version of the ADSP-2100 DSP Microprocessor, introduced in these pages in 1986 (*Analog Dialogue* 20-2). Fabricated in a 1.0-μm CMOS process, the new 12.5-MHz ADSP-2100AK and 10-MHz ADSP-2100AJ join the 8- and 6-MHz ADSP-2100K and J. This extended family makes available the ADSP-2100's code, instruction set, and all of its architectural advantages in a choice of speeds, packages, and prices. Military grades are also available. Packages include the 100-lead ceramic pin-grid-array (G) and a 100-lead plastic quad flat pack (P). Prices start at $78 in 1,000s (ADSP-2100JP).

The ADSP-2100/2100A contains (Figure 1) a multiplier/accumulator, arithmetic-logic unit, shifter, two address generators, a program sequencer, and an instruction cache—plus registers, internal buses, feedback connections, and buses that provide independent (simultaneous) access to a pair of external data and program memories. The program memory can also store data, which is accessed in parallel with the data memory while the internal cache provides instructions.

A DSP microprocessor's performance depends on both its cycle rate and what it can accomplish per cycle. The 56% increase in clock speed of the ADSP-2100AK over its powerful predecessor is thus only part of the story. The ADSP-2100/2100A's parallel architecture is designed to make each cycle highly productive. In a single cycle it can *simultaneously*: perform a computational operation (MAC, ALU, or shift), generate the next program address and fetch that instruction, perform one or two data transfers, and update one or two address pointers.

Combining this faculty with its increased speed, the ADSP-2100A can perform a 1,024-point complex radix-4 FFT in 3.0 ms, faster

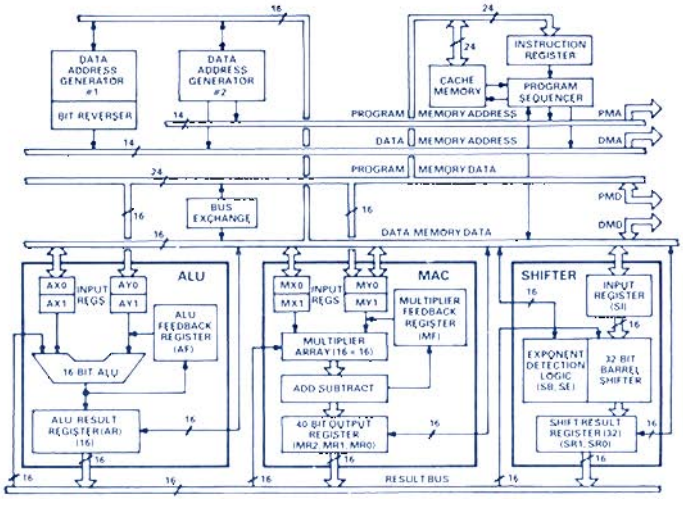
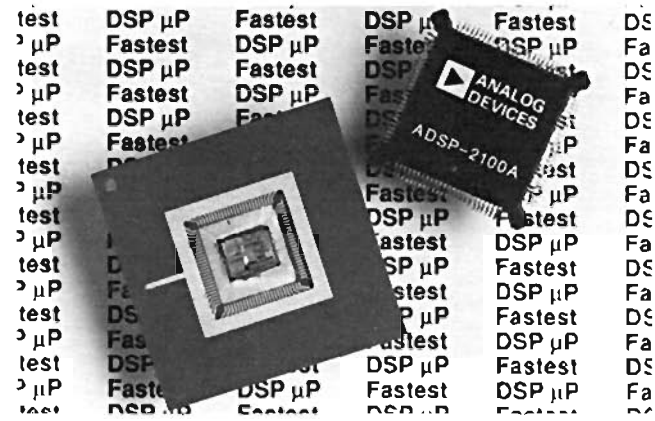


Figure 1. Basic architecture of the ADSP-2100. The independent MAC, ALU, and barrel-shifter sections – plus the dual bus and addressing structure, the internal R-bus, and instruction cache – are central to its processing power.

*For technical data, use the reply card. If you wish to see copies of the various Manuals: *User's*, *Applications*, *Cross-Software*, and *Evaluation-Board*, get in touch with your local sales office.



than any of today's general-purpose DSμPs—and approaching the speed of dedicated FFT chips.

The ADSP-2100/2100A includes among its important features:

- Single-cycle access to large external memories: 16K×16 of data memory and 32K×24 of program memory (16K instructions and 16K additional data). Data can be accessed in *both* memories within a single cycle.
- The "virtual" three-bus architecture that is supported by the 16-instruction cache memory is automatically used in program loops typical of DSP algorithms; it allows two external data accesses in parallel.
- The powerful program sequencer makes available zero-overhead looping for efficient implementation of DSP algorithms, single-cycle ("immediate") branches for speed and simplified programming, and sophisticated interrupt processing for quick and painless response to external conditions.
- Easy-to-use software tools are available for PC/MS-DOS, VAX/VMS, and UNIX; they include cross-software modules, including Assembler, Linker, and Simulator, and an ANSI draft standard C Compiler. In addition, an available stand-alone evaluation board executes signal-processing algorithms *in real time*; with it, engineers and programmers can run simulations before committing to a final production design (see photo).

The ADSP-2100A scaling was engineered by Dan Essig, with layout by Dennis Hillstrom; The Evaluation Board—and the ADSP-2100 Emulator—were designed by Kevin Leary. All are in ADI's Digital Signal Processing Division, in Norwood MA.

CMOS VIDEO DACS PROVIDE MEMORY, INTERFACE, 3 OUTPUTS

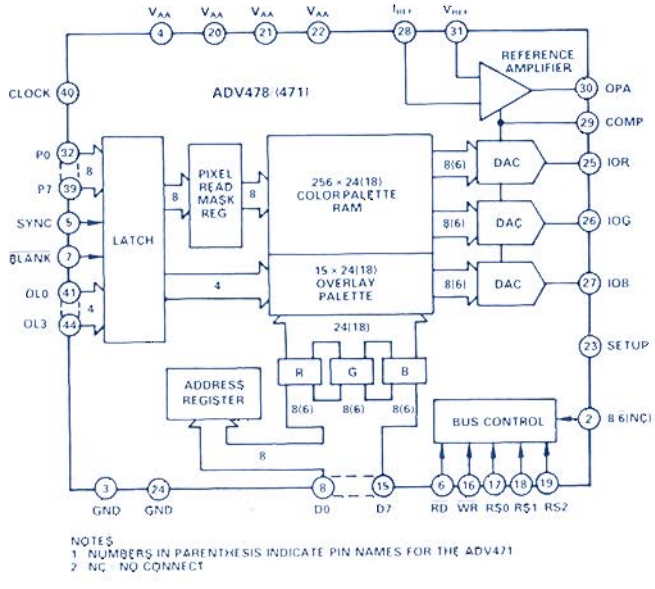
ADV478 (8-Bit) and ADV471 (6-Bit) Provide 256 Colors Support Color Overlays, Drive CRT Amplifiers Directly

The ADV478* and ADV471 monolithic triple video DACs—fit-, form- and function-compatible equivalents of the Bt478 and Bt471—are designed to act as the interface between computer graphics memory (such as in the VGA graphics of an IBM Personal System/2®) and the electron gun drivers of a color CRT. Both devices contain three DACs (for red, green, and blue primary colors), RAM for color lookup tables, separate memory for special color overlays, and output circuitry. Also included are support circuits and processor-bus interfacing circuits.

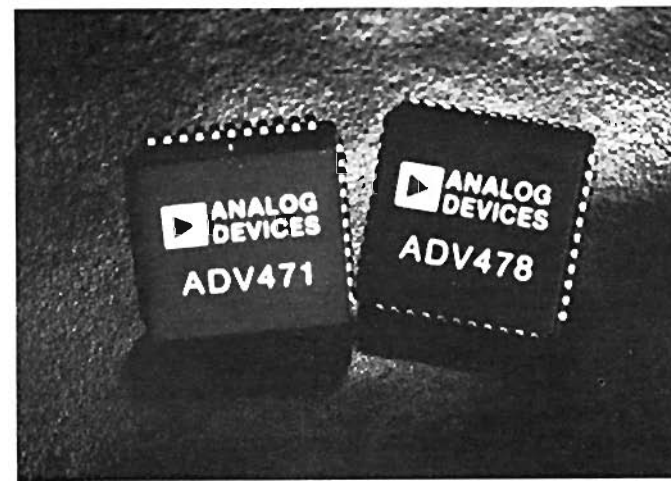
The ADV478 and ADV471 are pin- and software-compatible and differ only in the number of bits allocated for each color. The ADV478 can be configured for either 8-bit (256 intensity levels per color) or 6-bit (64 levels) operation. The ADV471 has only 6 bits, (64 intensity levels) per color. The devices' various grades will support clock rates of 35, 50, or 80 MHz; higher clock rates are needed to refresh higher-resolution displays often enough to prevent perceived image flicker. A 35-MHz rate is suitable for 768 × 576 pixel resolution; 80 MHz gives 1,000 × 1,200 flicker-free pixels.

The ADV478 can display *any* 256 colors (out of 16.8 million), via a 256 × 24-bit internal color-palette RAM. The RAM's 24-bit output supplies the 8-bit intensity code for each of the three DACs. The ADV471's internal color palette is also 256 words deep, with each word 18 bits wide, for a universe of 262 thousand color choices. Under program control, the colors in the palette can be changed as needed; they can also be read back by the graphics program using a *read* command. The palette's colors can be any subgroup from the total universe: e.g., all shades of a single color, or fewer shades of some colors plus specific single-shade colors.

Both devices support *overlay registers*. A special 15 × 24 bit RAM



Block diagram



in the ADV478 (15 × 18 bits in the ADV471) holds color information for screen overlays—cursors, grids, and menus—that should appear in programmed colors, regardless of the screen graphics. With these priority registers, 15 additional colors can be displayed independently of the main color palette and without overwriting the palette colors; this simplifies software and reduces the number of color-palette rewrites that must be executed.

The DACs are interfaced to the processor bus via a standard 8-bit microprocessor interface, which operates asynchronously to the high-speed pixel clock. Data transfers between internal registers are synchronized by internal logic; they occur between μP accesses. The color-palette RAM and overlay registers can be accessed at any time without causing visible glitches on the display.

DAC Outputs The external full-scale reference for the DACs can be either voltage (1.2-V nominal) or current (−3 to −10 mA). A single resistor sets the relationship between the reference value and full-scale output level. A bit in the setup-control word indicates whether a 0 IRE or 7.5 IRE blanking pedestal (the amplitude difference between black and retrace blanking) should be used. The span from blanking to full intensity is divided into 100 IRE (Institute of Radio Engineers) units; most signal levels are quantified in terms of these units.

Video outputs are high-impedance current sources that are RS-343A compatible and can directly drive a doubly terminated 75-Ω load (37.5-Ω equivalent impedance); they are also RS-170 compatible for singly terminated 75Ω loads. All three DAC outputs provide sync at −40 IRE, along with the analog color output. Maximum differential and integral linearity errors are ±1 LSB for the 8-bit AD478 and 1/4 LSB for the 6-bit ADV471, over the entire 0 to +70°C operating temperature range.

The ADV471 and ADV478 are packaged in 44-pin PLCCs. Typical power dissipation for these +5-V CMOS devices is <800 mW. Prices for the ADV471 and ADV478 are $29/$36/$57 and $41/$51/$89 (100s) for 35/50/80-MHz versions.

*Use the reply card for technical data.

MONOLITHIC 12-BIT QUAD READBACK DAC SAVES BOARD SPACE

The AD664 Offers Voltage Output, Four-Quadrant Multiplication Choice of Features in Two Packages: 44-Pin LCC and 28-Pin DIP

The AD664* is a monolithic chip (Figure 1) with four complete 12-bit voltage-output multiplying d/a converters that share a bi-directional microprocessor interface. Monolithic multiple DACs provide savings when many high-resolution voltage-output DACs are needed for systems applications in which reliability is paramount and board space, power dissipation, and design effort are costly; examples include automatic test equipment, avionics, I/O boards for PCs, robotics, and high-end disk drives.

The analog portion of the AD664 (Figure 2) consists of four DAC cells, four output amplifiers, a control amplifier, and switches. The output range of each DAC cell is independently programmed through the digital I/O port (LCC-packaged units) and may be set to unipolar or bipolar range, with a gain of 1 or 2 times the reference voltage; with a +10-volt reference, ±15-volt analog supplies, and a +5-volt logic supply, the specified output ranges are 0 to +10V, −5 to +5 V, −10 to +10 V.

The AD664 is available in two sets of versions, a 44-pin LCC ("E") package with all functions described here—and a 28-pin ceramic DIP ("D" package) with dedicated unity gain and optional unipolar (*UNI* , 0 V to + V_{REF}) or bipolar (*BIP* , $\pm V_{REF}$) range. In addition, the "D" versions have a 12-bit I/O data buffer, for 12- or 16-bit buses, while the "E" versions' three 4-bit nybbles allow them also to communicate with 4- and 8-bit buses.

The AD664's multiplying DACs permit the use of a common positive-or-negative fixed-or-variable external reference; for example, the system reference of an ATE system. All four DACs guarantee ±1/2-LSB max integral and differential nonlinearity at 25°C—and monotonic performance with ±3/4 LSB max integral nonlinearity over the rated temperature range. Maximum gain error is ±5 LSB, with a gain tempco of ±10 ppm of full-scale range/°C. Unipolar offset error is ±1 LSB, and bipolar zero error is ±2 LSB, with tempcos of ±2 ppm/°C and ±10 ppm/°C. DAC-to-DAC matching and tracking specifications are comparable.

Each DAC has a double-buffered input latch structure, which

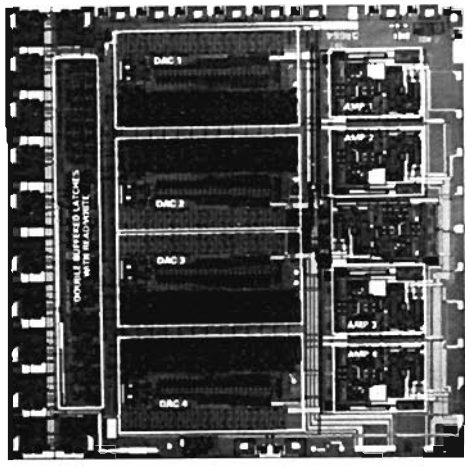
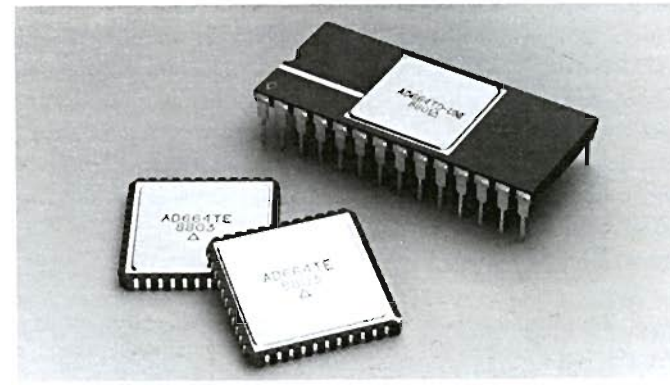


Figure 1. Chip photo of the AD664.

*Use the reply card to receive a free 20-page data sheet.



permits simultaneous update of one—or all four—DACs, and a data-readback function. All DAC *read* and *write* operations are conducted through a single microprocessor-compatible I/O port. The choice of 4-, 8-, or 12-bit parallel lines ("E" versions) allows simple interfacing with a wide variety of microprocessors. A *reset-to-zero* control pin is provided to allow a user to set all DAC outputs to zero simultaneously, regardless of the contents of the input latch. Any one, or all, of the DACs may have both ranks of latches placed in a *transparent* mode ("E" versions), allowing the outputs to respond immediately to the input data.

Operating from ±12-volt to ±15-volt (and +5-V) supplies, the AD664 typically dissipates 400 mW. It is specified for operation over two temperature ranges, −40 to +85°C (AD664BD-UNI, AD664BD-BIP, and AD664BE), and −55 to +125°C (AD664TD-UNI, AD664TD-BIP, and AD664TE, all available to MIL-STD-883B). Prices start at $60.80 in 100s (AD664BD-UNI).

The AD664 was designed by Steve Lewis at Analog Devices Semiconductor, Wilmington MA.

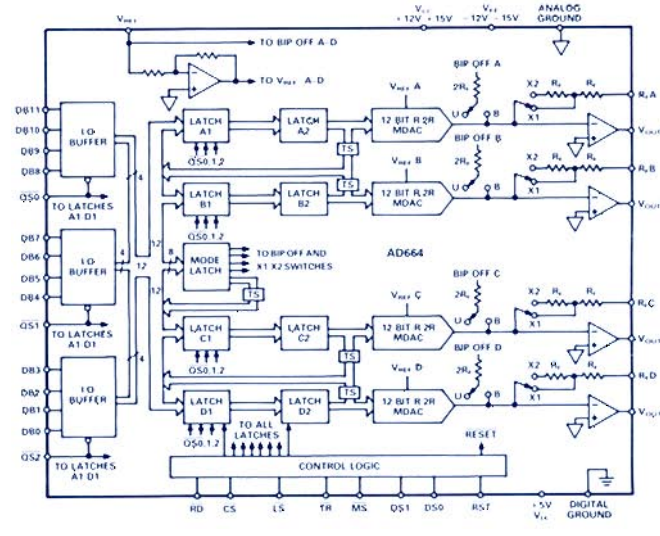


Figure 2. Block diagram of AD644's versatile 44-pin LCC "E" version. The dedicated 28-pin-DIP "D" versions have a 12-bit broadside data interface; unipolar and bipolar fixed-gain output options are available.

VOLTAGE-TO-CURRENT ISOLATOR PROVIDES HIGH ACCURACY

1B21 Provides 1,500-VRMS Isolation in a Small Package at Low Cost
Device Has Programmable 4-20 mA and 0-20 mA Ranges

The 1B21* voltage-to-current (V/I) converter provides isolation to ±1,500 V rms in a small, low-cost package using surface-mount technology. It is intended to protect the signal source in process-control applications that require electrical isolation between the source, e.g., programmable-controller output, and the load (typically a valve or actuator) controlled by this source.

The 1B21 receives a high-level signal voltage, ranging up to 0 to +10 V, and converts it to a 0-20 mA or 4-20 mA output for a control loop. The input section of the 1B21 is powered by a ±15 V supply, while the output loop uses a separate local or remote supply. Magnetic coupling techniques achieve high isolation with low nonlinearity, typically ±0.02% (±0.05% max). The small size of this module is advantageous—and necessary—for high-density multi-channel printed-circuit board designs.

Similar in concept and technology to the AD202/AD204 series of isolation amplifiers (*Analog Dialogue* 20-1), the 1B21 has three functional sections: a programmable inverting amplifier for the signal input, an isolation barrier, and a modulated current source (Figure 1). The gain and offset of the input amplifier are set by two external, user-supplied resistors. Any range from 0-1 V to 0-10 V can be selected (for example, 1-5 V), either from a table or by simple calculations.

The scaled and conditioned input signal modulates a carrier to produce a square wave of peak-to-peak amplitude proportional to the input signal. This signal is applied to the signal transformer, which is specified to provide isolation to 1,500 V rms and ±2,000 V dc, continuous. The isolation, which also eliminates ground loops, meets IEEE Standard 472 (Surge Withstand Capability) for Transient Voltage Protection (±2,500 V peak CMV).

After passing through the signal transformer, the signal is demodulated and filtered using a single-pole filter. This filter's output provides the current-control signal for the output stage. The output current source draws excitation from an external supply in series with the load, completing the loop.

Power for the output-side circuitry of the 1B21 (except for the current loop) is provided by a rectified signal generated by a transformer-isolated 25-kHz oscillator (on the input side); it also provides timing information for modulation/demodulation.

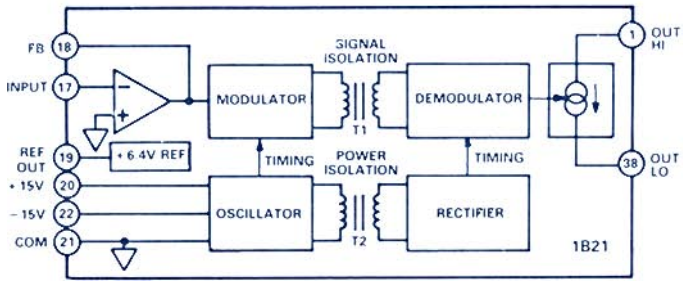
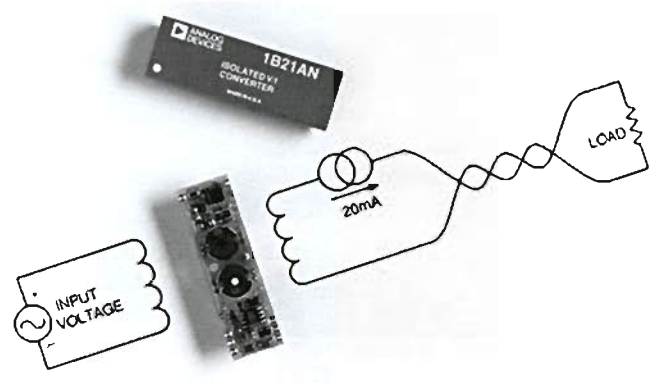


Figure 1. Block diagram

*Use the reply card for technical data.



Output range, of either 0-20 mA or 4-20 mA, is determined by the value of an external resistor. The loop supply is typically +24 V dc but can range from +15 to +30 V; because the 1B21's output is only 25 mA for input saturation, the supply need be rated for only 25 mA. Compliance is 27 V with the +30 V supply, which allows the 1B21 to drive ≤1.35-kΩ loads. An internal 6.4-V reference, with a ±20 ppm/°C temperature coefficient, is provided to develop the 4-mA offset required for the 4-20 mA range.

1B21 modules can share a circuit board, providing multiple-channel outputs for analog signals. If the output circuits have a common connection, a single loop-supply can be used for all channels (Figure 2), as long as the supply can furnish 25 mA per channel. With a single supply, the *output* channels are not isolated from one another, but in such applications isolation achieves the objective of protecting data acquisition systems on the input side from damage by output-side transient voltages.

The high accuracy of the 1B21 is indicated by the low output offset and gain temperature-coefficients, ±300 nA/°C and ±50 ppm/°C FSR, respectively. Small size (0.7 × 2.1 × 0.35 inches, 18 × 53 × 8.9 mm) provides a new level of price and functional density in a single, easy-to- apply package. The 1B21 is priced at $39 each in quantities of 100 pieces.

The 1B21 was designed by Alan Jeffery, at the Analog Devices Interface Products Division, Norwood MA.

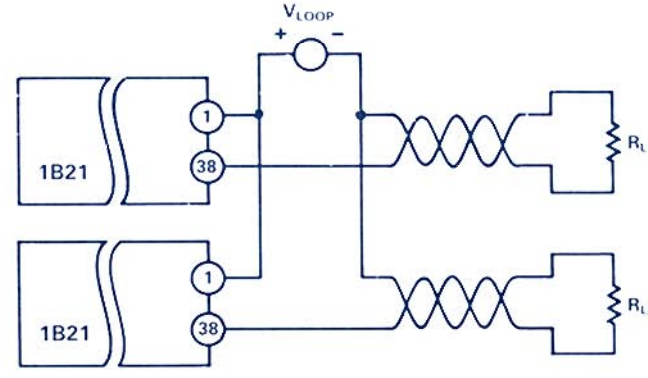


Figure 2. Multiple 1B21s with a single loop supply.

AD652: IMPROVED MONOLITHIC SYNCHRONOUS V/F CONVERTER

0.005% max Nonlinearity to 1 MHz Full Scale; 0.02% at 2 MHz FS

Pin-Compatible with VFC100; Has Accurate 5-V Reference Output

The AD652* is a fast, high-precision single-chip analog (voltage or current)-to-frequency converter. It is *synchronous*, in that its full-scale output frequency depends on an external clock instead of the period of a one-shot oscillator. Its many applications include analog-to-digital conversion, signal isolation, analog-signal multiplexing, transducer interfacing, frequency-to-voltage conversion, frequency multiplication, and delta modulation.

The AD652 has low ±0.005% maximum nonlinearity for full-scale frequencies up to 1 MHz, increasing to ±0.02% maximum at 2 MHz. The high clock rate, combined with the low nonlinearity, facilitates high-speed, high-accuracy a/d conversion; at 2 MHz full-scale (4-MHz clock), the AD652 can perform a 16-bit a/d conversion in 32.77 ms (Figure 1). The AD652 contains a +5-volt reference that can supply up to 10 mA (over temperature) to an external load, such as a bridge transducer, for direct sensor-to-digital conversion. It is accurate to within ±25 mV, ±50 ppm/°C max in KP/BQ versions.

The AD652's basic frequency-voltage relationship is:

$$f_{OUT} = \frac{V_{IN}}{10V} \cdot \frac{f_{CLOCK}}{2}$$

for 10-volt full-scale input. By employing an external clock (which may be crystal-controlled) to set its full-scale frequency, $f_{CLOCK}/2$, the AD652 eliminates the need for critical timing components, such as expensive precision capacitors. This reduces maximum gain drift to ±25 ppm/°C and ensures a low ±0.5% maximum gain error. Because synchronous operation makes multiplexing easier, the AD652 is a powerful tool in multichannel data acquisition.

The AD652 is pin-compatible with the AD651 [*Analog Dialogue* 20-2] and VFC100 synchronous VFCs; it is also more accurate and less expensive. Additional features not found elsewhere include PLCC packaging with on-chip application resistors for space-critical designs (Figure 2), and an optional offset trim capability to improve accuracy beyond rated specifications.

Available in 20-terminal PLCC ("P") and 16-pin Cerdip ("Q"), the AD652 is available in five grades and specified over the 0 to +70°C (JP, KP), −40 to +85°C (AQ, BQ), and −55 to +125°C (SQ) temperature ranges. The JP/AQ/SQ guarantee these maximum specs: ±1% gain error, ±50 ppm/°C gain drift, and ±0.02% maximum nonlinearity at 500 kHz; the KP and BQ's max specs include ±0.5% gain error, ±25 ppm/°C gain drift, and ±0.005% nonlinearity at 500 kHz. Prices start at $6.95 (100s).

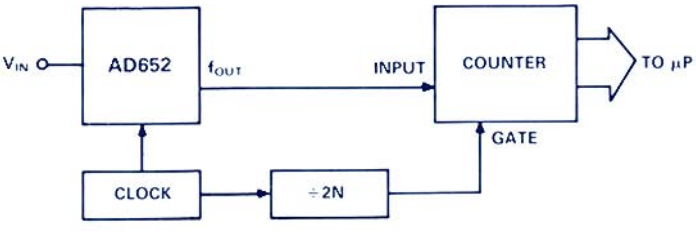
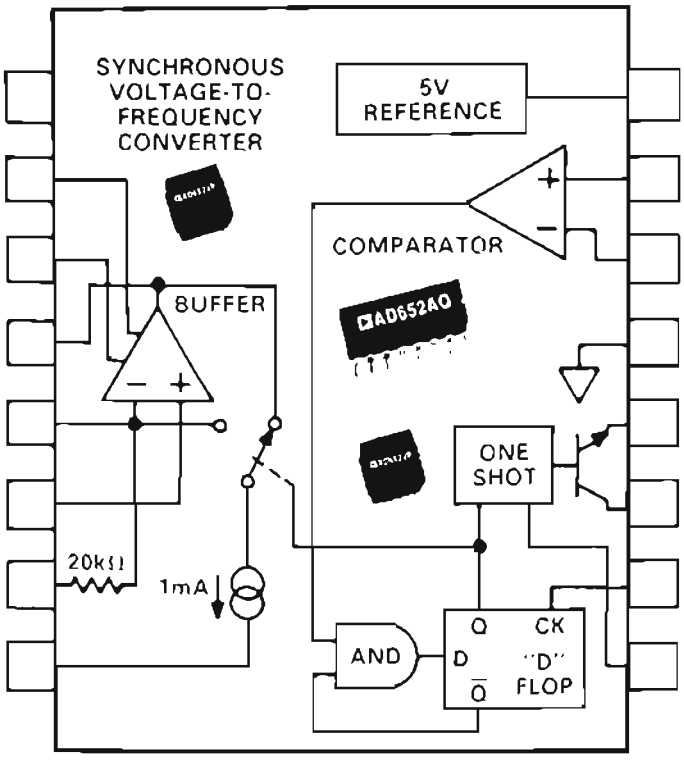


Figure 1. A/D converter using a synchronous VFC.

*Use the reply card to obtain a free 16-page data sheet.



The AD652 was designed by Larry DeVito at Analog Devices Semiconductor, in Wilmington MA.

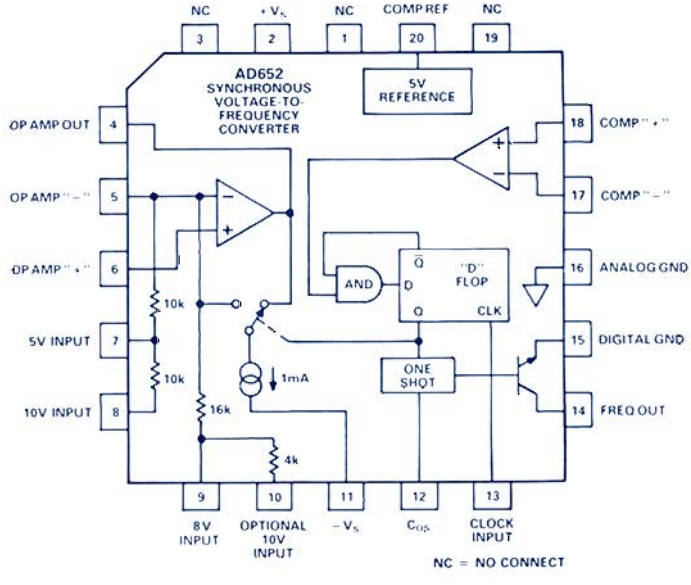


Figure 2. Block diagram of PLCC version. Note additional scaling resistors.

12-BIT MONOLITHIC ADC GUARANTEES 3-μs CONVERSION TIME

CMOS AD7672 Uses +5, −12-Volt Supply, Handles Unipolar & Bipolar Data Has Fast Bus Access: 90 ns; Packaged in LCC, PLCC, and "Skinny" DIP

The AD7672* is a monolithic CMOS high-speed successive-approximation analog-to-digital converter capable of performing 12-bit conversions in 3 microseconds. It can handle both unipolar inputs (0 to +5 V and 0 to +10 V) and bipolar inputs (±5 V) with on-chip application resistors (Figure 1).

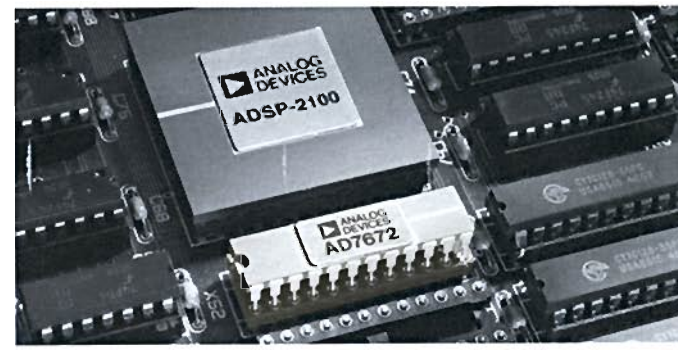
Its low 180-mW maximum power dissipation permits the AD7672 to be packaged in small 28-terminal leaded ceramic chip carrier (LCCC—"E") and plastic-leaded chip carrier (PLCC—"P") surface-mount packages, as well as skinny 0.3" 24-pin plastic ("N") or ceramic ("Q") DIPs. Designed for high-speed processing applications, the AD7672's 90-ns maximum bus-access time eliminates *wait* states when using high-speed processors such as the ADSP-2100, the TMS320C25, and the MC68020.

The AD7672 is a descendant of the AD7572, the industry's first 5-μs monolithic 12-bit ADC [*Analog Dialogue* 20-1]. For maximum flexibility (and improved accuracy and drift characteristics), an off-chip reference is used. For example, designers of wideband dc measurements can specify a precision device, such as the AD588* 1.5-ppm/°C monolithic reference (Figure 2); on the other hand, for ac signal processing applications, where offset and gain accuracies are less critical, a more ordinary reference can be used.

As Figure 2 shows, the AD588 is especially useful because it provides both the reference voltage and a precisely tracking bipolar-offset voltage for applications involving inputs in the range from −5 to +5 volts.

The AD7672 operates from +5-volt and −12-volt supplies; this makes the device convenient to use for applications in PC-based input/output systems, since a dc-dc converter is not necessary.

Available options include speed, accuracy, temperature range, and (as noted above) packaging. Its three speed versions are the AD7672XX03, -05, and -10, which guarantee maximum conversion times of 3.125, 5, and 10 μs with synchronous clocks of 4,



2.5, and 1.25 MHz—and 3.125±0.125, 5±0.2, and 10±0.4 μs with asynchronous clocks.

Specified operating temperature ranges are 0 to +70°C (K,L), −25°C to +85°C (B,C), and −55 to +125°C (T,U—05 and 10 suffixes only at present). Guaranteed maximum specifications for K/B/T grades over temperature include ±1 LSB integral nonlinearity, ±0.9 LSB differential nonlinearity, ±4 LSB offset error, and ±6 LSB gain error. Comparable specs for the L/C/U grades (over temperature) include: ±1/2 LSB integral nonlinearity (±3/4 LSB for U grade), ±0.9 LSB differential nonlinearity, ±6 LSB offset error, and ±7 LSB gain error. Prices start at $33/$44/$75 (100s) for the 10/05/03 versions.

The AD7672 has a 12-bit parallel interface, with three-state data outputs and standard microprocessor control inputs (Chip Select and Read). The on-chip clock oscillator may be used with a crystal resonator for accurate definition of conversion time. The clock input may also be driven from an external source, such as a microprocessor clock.

The AD7672 was designed by ADI Fellow Mike Tuthill, at Analog Devices BV, Limerick, Ireland.

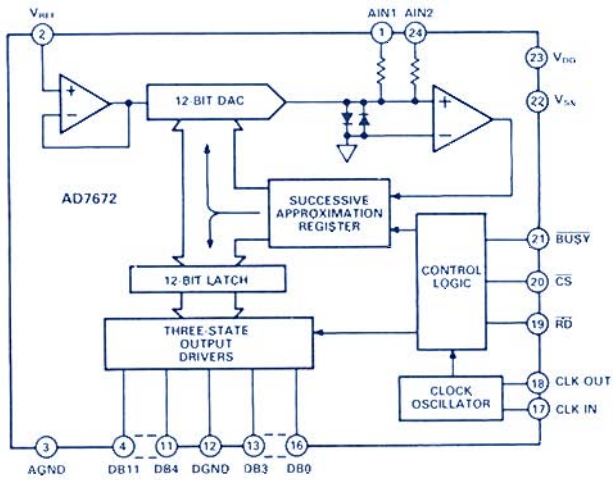


Figure 1. Functional block diagram

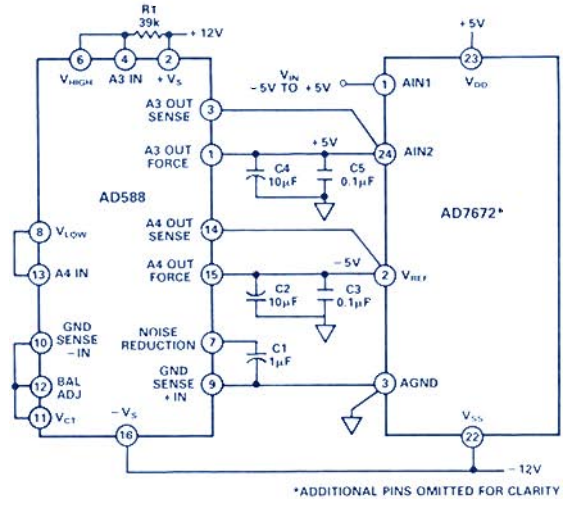


Figure 2. Bipolar operation using an AD588 reference. The bipolar-offset voltage is applied to AIN2.

*For complete technical data, use the reply card.

CHOOSE VMEbus VIDEO DIGITIZER BOARDS TO MATCH SOURCE

RTI-684-HS Supports Eight RS-170 Inputs, Has RGB Output

RTI-683-HS Supports Non-RS-170 Cameras and Sensors

For VMEbus-based systems used in video applications, two plug-in boards in the RTI-680 Series provide a wide range of video signal options. The RTI-684-HS*, for RS-170-compatible inputs, and the RTI-683-HS*, for other video inputs (Figure 1), provide features common to all video digitizing applications yet differing substantially between RS-170 and other environments.

RTI-683-HS: TV cameras generally have output formats defined by the RS-170 standard. However, many industrial and scientific sensors create images with line and frame signals and rates that are not RS-170-compatible. Line-scan and area sensors, using linear and square arrays, provide video information in formats that are much more varied and flexible than RS-170 allows. The RTI-683-HS, a programmable asynchronous input module, digitizes images with a gamut from low resolution/fast frame rates to very high resolution/slow frame rates.

The line length and the conversion rate are fully programmable. Slow imaging devices, for example, scanning electron microscopes, and fast image devices—such as radar scanners—can be accommodated with a pixel conversion rate up to 10 MHz and maximum resolution of 8 bits. The conversion rate can be slaved to the sensor sampling pulse, if necessary, or a clock within the RTI-683-HS can be used. The range of image resolutions spans 1 × 1 pixel to 4,096 × 4,096 pixels, with frame rates from 0.1 to 1,000 frames per second.

To minimize noise in the digitized image—most often a problem in slow-scan images—digital block-average circuitry is included; it averages many samples to produce an accurate pixel value despite the noise. Each of the 4,096 pixels on a line has separately determined digital gain and offset settings; this provides the ability to calibrate and compensate for nonuniformities in both sensor and ambient lighting.

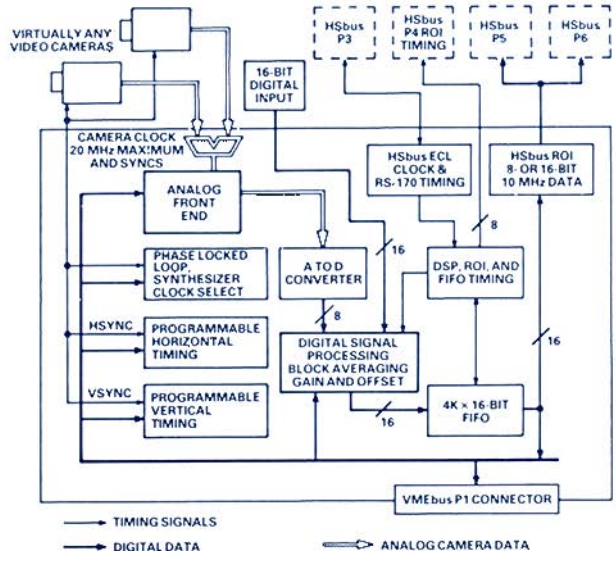
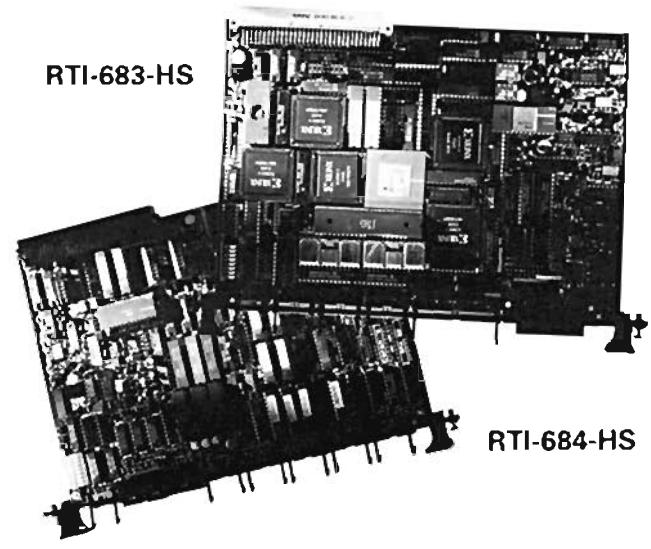


Figure 1. RTI-683-HS subsystem for non-RS-170 signals.

*Use the reply card for technical data.



Many imaging applications require locating the edge transitions of the image and ignoring the broad, unchanging areas of the image. For these applications, a horizontal run-length encoder with programmable threshold is available to store the positions of gray-scale transitions. This produces a compressed-data version of the image, requiring less memory space to store and greatly reduced bus time to transfer to the host CPU.

RTI-684-HS: Unlike the variety of sensor formats that non-RS-170 devices supply, many video-output devices (such as TV cameras) provide signals in the "broadcast-originated" RS-170 format, either directly or in emulation. The RTI-684-HS board (see photo) can accept any one of eight RS-170 inputs, selected under software control. Each input is passed through a sync stripper, one of four selectable filters (for anti-aliasing and noise reduction), and dc-level-restoration circuitry. A programmable-gain amplifier and offset circuitry further condition the video signal.

The resulting signal is then digitized, to 6- or 8-bit resolution—for further analysis by the host CPU and for creating an RS-170 video output. This RGB (red-green-blue) output is generated by digital values entered into three color output look-up tables, which feed three d/a converters to drive standard color monitors.

Both of these VMEbus-compatible video digitizing boards can transfer data to other system boards over the VMEbus itself or via a high-speed, private bus which provides timing, handshaking, and data paths for transferring large blocks of data at high rates (often necessary in image-processing applications).

The RTI-683-HS non-RS-170 board is a 16-channel digital (D16), 24-channel analog (A24), VMEbus slave; it looks like a 64-K byte block of memory. The RS-170 board (RTI-684-HS) is a D8, A24 slave device, configured as a 16-byte memory block. Prices are $3,995 and $2,475, respectively.

DATA ACQUISITION & CONTROL SOFTWARE FOR PC PLUG-INS

Menu-Driven Control EG: High Point-Count, Functionality, Graphics, Directly Supports RTI-800 Series Boards, 3B/5B Modules

Control EG*™ provides industrial and laboratory users of IBM PCs (and compatibles) with flexible, powerful menu-driven data-acquisition and control capability. Up to 256 I/O points per PC—up to 160 of them analog—can be handled, using multiple plug-in boards (a single RTI-820 board can support 64 analog I/O points). The system operator can call up a variety of screen displays of data and results (Figure 1)—historical data, X-Y plot, annunciator panels, bargraphs, text, logs, or sequence-of-events.

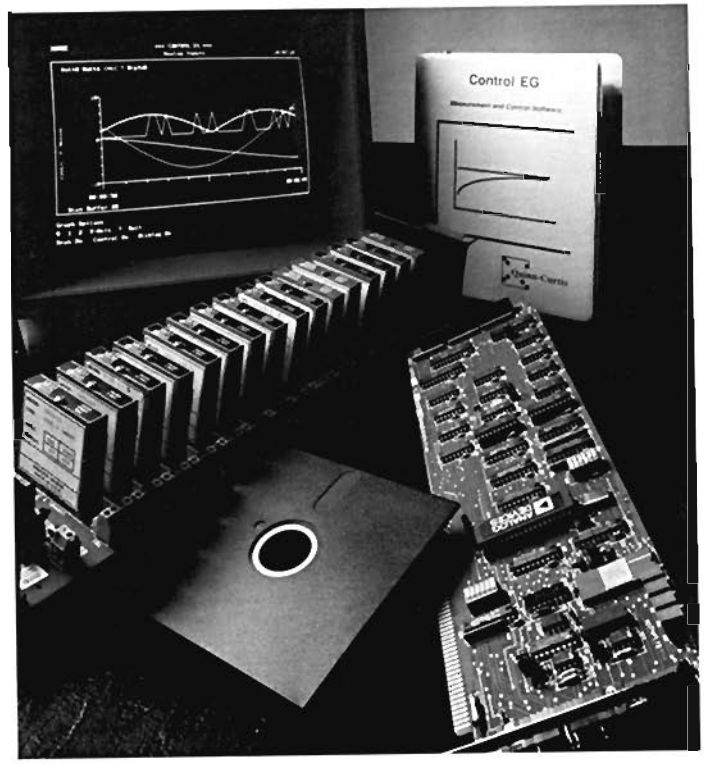
Designed for use with the RTI-800 and 3B/5B series of analog and digital I/O boards and signal conditioning modules, Control EG's software functions can acquire data, analyze it, and present it in a variety of formats. Control EG can also control a process automatically throughout its entire cycle. Under program control, it can open and close valves, change and ramp set-points, modify channel-scanning rates, log data to disk, and activate a printer.

In a typical measurement-and-control loop, the sensor signal (e.g., thermocouple voltage) cannot be used directly by the system computer. Weak signals must be amplified and (often) isolated, scaled to the proper range, and linearized. Control EG works closely with the 3B and 5B series of signal conditioning modules that precede the RTI-800 series I/O board. The user types in the signal-conditioner model number, and the software looks up the proper scaling and linearization factors in built-in tables. The result is scaled in engineering units (e.g., volts, degrees).

Users can also define calculated variables, mathematical or logical functions of analog or digital inputs, entered as algebraic or Boolean equations. Results can be displayed and logged like inputs.

Software for the most common closed-loop control algorithm, PID (proportional + integral + derivative, relating the manipulated variable to the error), is built into Control EG, for up to 32 independent loops. The operator enters setpoints and coefficients (gain, reset rate, derivative rate); the loop runs automatically.

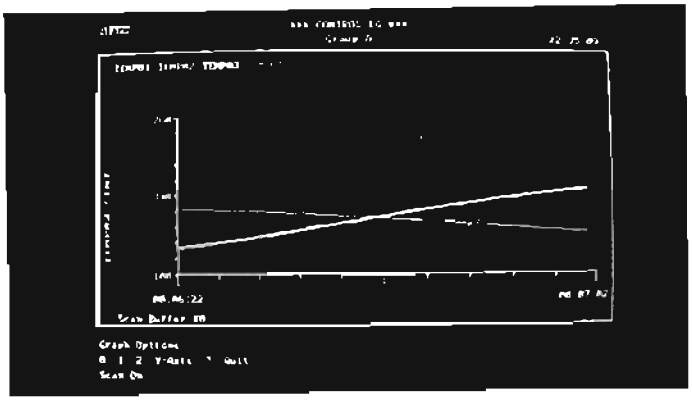
When the system is programmed for alarm scanning for high and low input values, at up to 64 ch/s on an IBM PC AT, any alarms



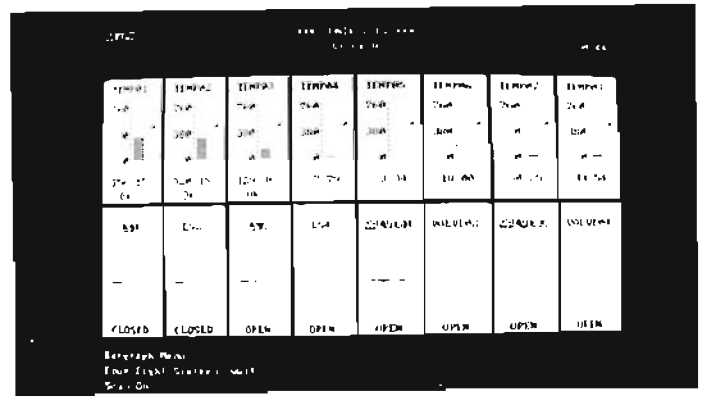
that occur are logged; user-defined messages appear on the screen.

In setting up Control EG, Configuration Tables define hardware (which board, which location), input and output channels, desired calculations, alarm limits and messages, sequence of up to 8 different events, variables to be graphed (and format), and run-time parameters, e.g., scanning and update rates. The user selects what the screen displays: real-time or saved data, and whether to alternate. A spreadsheet-compatible format aids further analysis.

Furnished complete (no "add-ons" needed), Control EG comprises 2 disks, a comprehensive user's manual, and a single-use or site-licensing agreement. Single-use cost is $500.



a. History display shows past data for multiple signals versus time.



b. Data from multiple channels displayed in real time, with process control faceplate format showing variable name, alarm limits, setpoint, and present value.

Figure 1. Control EG screens.

*Specify AC1904; use the reply card for technical data.
™Trademark of Quinn-Curtis, Inc.

NEW ENHANCEMENTS TO LTS-SERIES OF BENCHTOP IC TESTERS

High-Accuracy Op-Amp Family Board, VAX and PC Networking, and Component Manipulator Increase LTS-2020's Capabilities

The LTS-2020* Component-Test System family can test linear, digital, data-conversion, and discrete devices in a convenient menu-driven, BASIC-programmable instrument. Included in the LTS-2020 system are RS-232 and IEEE-488 ports, dual disk-drives for test-program and data storage, automatic self-calibration, and software for statistical analysis. LTS-2020 systems are used in both the engineering lab and incoming inspection.

Enhancements* to the LTS-2020 benchtop component tester series expand its ability to test precision devices, improve its networking capability, and increase its device-handling productivity:

- an Op Amp Family Board, the LTS-2101, designed for testing high-accuracy, high-precision linear devices
- software packages in the 2020NET series for networking to DEC VAX, microVAX, and IBM PC systems
- The LTS-1536 manipulator for mechanically interfacing the LTS console to probers and handlers.

The LTS-2101 Op Amp Family Board is a significant improvement over the LTS-2100, its predecessor. It can test offset voltage with accuracy to within $\pm(0.25\% + 5\mu V)$, necessary for comparators, voltage regulators, and low-offset op amps. For FET-input op amps with sub-picoamp bias currents, the LTS-2101 can measure current with error less than $\pm(5\% + 25\ fA)$.

Several precautions minimize measurement-induced errors: A multilayer printed-wiring board, careful grounding, and 0.5-μV-thermal-EMF relays in the switching matrix reduce errors caused by ground loops and thermocouple effects. Test times are reduced by a "pulse load ready" signal, which is polled by the test program to check whether the capacitor for the pulse load is charged. The test-loop gain is greater than 10,000 for the high resolution needed when amplifying small signals.

All software developed for the existing LTS-2100, including program libraries, is compatible with the LTS-2101 hardware. Documentation includes instructions for creating test programs with "merge" software, information about low-leakage testing, schematics of family boards and socket assemblies, and BASIC-programming information. All standard op amps can be handled by this board, including dual and quad devices, 8-pin mini-DIPS, 14-pin DIPs, and a variety of TO metal can packages.

In addition to the basic board, accessories and socket assemblies are available. The LTS-2101 is priced at $4,000.

The 2020NET series of networking software is intended for DEC VAX/microVAX II computers or IBM PC (and compatible) systems. It allows data and programs in ASCII files to be transmitted via a bi-directional RS-232 port for uploading and downloading between a host computer and an LTS-2020 tester or LTS-2020 Test-Development station (*Analog Dialogue* 21-1) .

In a typical application, the host stores a sequence of setup procedures to be sent to the LTS-2020 for automated operation of the system. The LTS-2020 uses the host computer's hard disk to store test data and test programs. This reduces the need to save test programs on separate floppy disks, minimizes intervention by the operator, and provides overall system flexibility. The greater processing capabilities of the host computer can be used for correlation of data and test results, as well as central program library maintenance and revision control.

The 2020NET VAX-based networking software allows up to twelve LTS-2020s to be connected to a single multitasking VAX or microVAX; the PC-based system connects a PC to a single LTS-2020. Price for 2020NET depends on the host computer and magnetic media required. The range is from $1,500 to $2,000,

The LTS-1536 Reid-Ashman Manipulator is designed to provide a mechanical interface between automatic handlers and probers and the LTS-2020. The manipulator eases movement of the system console; it requires little time to set up on the test floor. Its power-assist reduces the console's "effective" weight to 20 pounds, so that little effort is needed to position the console; setup times are shortened and production throughput increases.

Positioning capabilities of this manipulator include up/down, side-to-side, in/out, and rotation around a side-to-side axis. Cumbersome mechanical locking of the interface cables is eliminated by the hard-docking feature, which improves cable and connector reliability while maintaining signal integrity due to the reduced distances between console and test head. Guide pins and latches prevent damage to contacts.

Accessories allow interfacing to the commonly used MCT automatic component handler (other interfaces are available; contact the factory for details). The standard LTS-1536 manipulator is priced at $5,950.

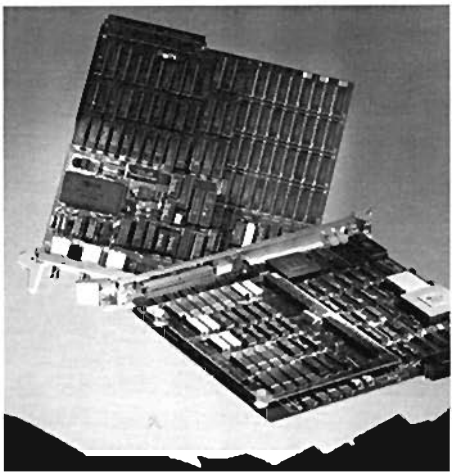
The LTS-2101 family board was designed by Jon Johnson and Paul Baginski at Analog Devices Component Test Systems (they are now at Analog Devices Semiconductor, Wilmington MA). The 2020NET software was designed by Nick Norman at CTS. ▶

*Use the reply card to request technical data.

8 MIPS Multibus II ARRAY PROCESSOR

16-Bit RTI-980 Is Based on the ADSP-2100 Chip

Development Tools Include Assembler, Linker, & Simulator



The RTI-980* Multibus II®-compatible Array Processor Board crunches numbers at up to 8 MIPS (million instructions per second) with 16-bit fixed-point format. It can compute algorithms for communication, signal processing, machine vision, and real-time data acquisition and analysis.

Speedy calculations are provided by the ADSP-2100 single-chip programmable DSP microprocessor, which features single-cycle instruction execution and incorporates an ALU, multiplier-accumulator, and barrel shifter; it works in conjunction with an 80188 microprocessor as an I/O processor, built-in self-test, and DMA support for a message-passing co-processor (MPC).

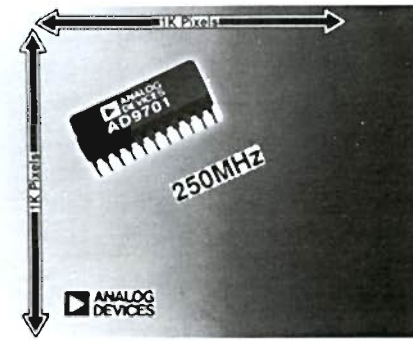
To communicate with other Multibus II boards in a system, the RTI-980 uses either the public bus or a high-speed private bus, supporting control signals, 20 address bits, 16 data bits, and data transfers at 8 MHz.

Software-development tools include an assembler, linker, and simulator for IBM PCs (MS DOS) and Intel iRMX286, plus target-environment tools. The RTI-980's price (1's) is $5,995.

8-BIT IC VIDEO DAC

250-MHz Update Rate

Low (60 pV-s) Glitch



The AD9701* is a high-speed monolithic 8-bit d/a converter with fully integrated composite video functions. It provides 8-bit updates at 250 MHz in synchronous operation. Applications include raster-scan & multicolor displays (one AD9701/color).

Built-in composite control functions—for composite sync and blanking, reference white level, and 10% bright level—minimize additional raster-scan logic requirements. The 250-MHz update rate supports CRT resolutions up to 1K × 1K pixels.

Features include 60 pV-s glitch impulse (critical in video applications), single-supply (−5.2-V) operation, with 728-mW typical power dissipation, and an internal voltage reference (for operation as a stand-alone video-reconstruction DAC). The video output setup level is adjustable through the control pin from 0 to 20 IRE units.

Two temperature ranges are available: AD9701BQ (−25 to +85°C), in a 22-pin ceramic DIP, and AD9701SQ/SE (−55 to +125°C), in either a ceramic DIP or a 28-terminal LCC. Prices start at $14 (100s).

TTL-COMPATIBLE 100-MHz 8-BIT FLASH ADC

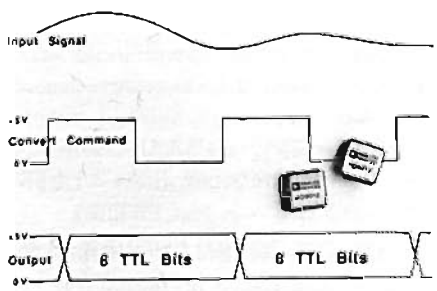
AD9012 Has Wide Analog Bandwidth, High SNR, Low Power

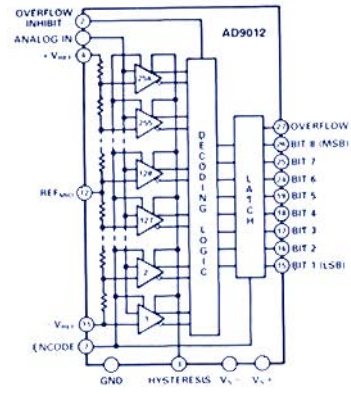
Low Input Capacitance Minimizes Demands on Input Buffer

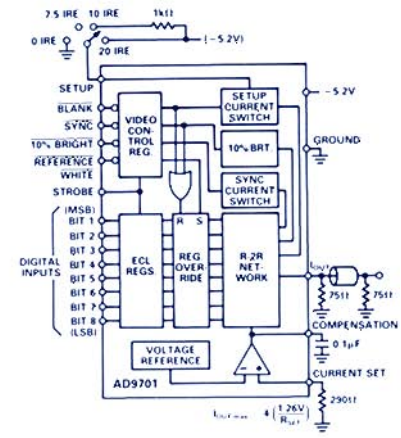
The AD9012* is an 8-bit monolithic flash converter with minimum full-scale sampling rate of 75 Msps (100 typical). A direct descendant of the 125 (150 typ)-Msps AD9002 (see *Analog Dialogue* 21-1), it has convenient TTL (instead of ECL) outputs. Typical applications include radar, digital oscilloscopes, digital radio, and electronic warfare systems.

The AD9012 has 16-pF input capacitance and 180-MHz analog bandwidth (for acquiring high-speed pulse inputs without an external track-and-hold). Signal-to-noise is greater than 46 dB, and harmonic suppression is 54 dB from dc to 1.23 MHz.

The AD9012's options include 0.5 or 0.75 LSB max nonlinearity, −25 to +85°C or −55 to +125°C operation, and 28-pin DIP or LCC package). An evaluation board is available. Prices (100s) begin at $70.





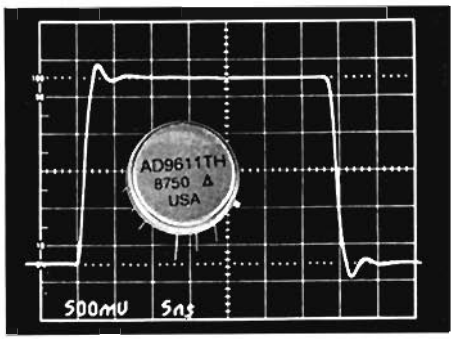


*Use the reply card for technical data.
†Multibus II is a registered trade mark of Intel Corporation.

New-Product Briefs

280-MHz OP AMP

AD9611: 7-ns 1% Settling Low Noise and Distortion



The AD9611* is a fast-settling, wide-bandwidth dc-coupled op amp combining high speed and dc precision. Designed for signal-processing applications requiring both high gain and wide bandwidth, it can be used as a buffer-driver for ADCs, an output amplifier for fast DACs, a photodiode preamp, and in many other ways.

It is designed as a *transimpedance* op amp: one whose error signal is current instead of voltage; because of this, its dynamic performance is essentially independent of closed-loop gain. Its −3-dB inverting bandwidth is > 250 MHz for closed-loop gains of up to 5 V/V and drops only to 200 MHz at a gain of 20.

Stable without compensation at unity gain, it settles to 1% in 7 ns—and to 0.1% in 13 ns. Rise and fall times are 1.3 ns and 1.5 ns, independently of the output step.

It is designed for wideband applications, but dc performance was not ignored. Input offset voltage is typically ±0.5 mV, with ±5 μV/°C drift; bias current at either input is ±1 μA, with drift of ±140/±75 nA/°C for the inverting/non-inverting inputs.

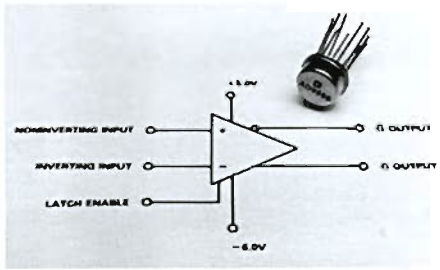
With ±5-volt supplies, its minimum output swing is ±2.8 V (at high temperatures, ±2.5 V), and it delivers a minimum full-range output current of ±40 mA. Available in two grades, BH (−25°C to +85°C) and TH (−55°C to +125°C), it typically dissipates 720 mW. Power dissipation remains constant as a function of load; this feature means that the AD9611TH can operate in ambients up to +110°C without needing a heat sink. Prices start at $84 (100s).

*Use the reply card for technical data.

TTL COMPARATOR WITH 7-ns PROP DELAY

High-Speed AD9686 Includes Complementary TTL Outputs, Latch-Enable Control Line; Uses Industry-Standard Pinout

The AD9686* is a monolithic TTL latching comparator with industry-standard pinout and only 7 ns of propagation delay. In addition to its complementary TTL outputs, the AD9686 provides a latch-enable control line —with 2-ns max setup time—for very high speed voltage comparisons.



With the capability to detect high-speed voltage transitions in both analog and digital systems, the AD9686 can be used for a variety of circuitry, including crystal- and RC-controlled TTL clocks, window comparators, peak and threshold detectors, and high-speed triggers and line receivers. Applications are found in input-range detection, high-speed analog and digital signal measurement, automatic test equipment, data communications, radar, EW, and missile guidance.

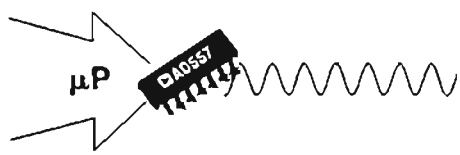
In addition to its high speed, the AD9686 has low input offset voltage: 2 mV max, with less than 10 μV/°C drift over the −25 to +85°C industrial temperature range and less than 13 μV/°C over the −55 to ±125°C military temperature range. Other key specifications include 4-μA input bias current and 85-dB common-mode rejection.

The AD9686 has comparable power dissipation to pin-compatible alternatives, 367 mW, maximum. It requires +5 and −6-volt power supplies and is available in a TO-100 metal can and a 16-pin hermetic ceramic DIP. The MIL-temp version is also available in a 20-terminal ceramic LCC. Prices start at $3.00 in 100s.

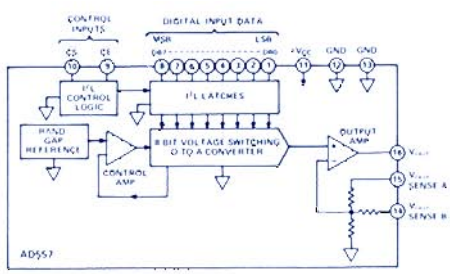
LOWEST-COST COMPLETE V-OUT 8-BIT DAC

AD557 DACPORT™ is Available in Skinny DIP or PLCC Operates from Single + 5-V Logic Supply

The AD557* is a complete monolithic 8-bit digital-to-analog interface. Guaranteeing monotonic behavior over temperature, it operates from a single +5-volt supply. On-chip functions include a complete double-buffered microprocessor interface, a bandgap voltage reference, and an output amplifier for driving loads directly.



It is designed and specified to produce any discrete 8-bit voltage in the full-scale range from 0 to +2.56 V (10 mV/bit) with a single +5-volt power supply. Dynamically, it settles to within ±1/2 LSB in 1.5 μs *max*. Its completeness and low cost make it an ideal upgrade for DAC08 in new designs and the most desirable choice wherever a true 8-bit monotonic bus-interfacing DAC must be powered by a single supply bus.



Additional *maximum* specifications of the AD557J include 1-LSB relative-accuracy error over temperature, full-scale error of ±2.5 LSB at 25°C (±4.5 LSB over temperature), and zero offset to within ±1 LSB at +25°C (±3 LSB over temperature).

The AD557J is available for 0°C to +70°C operation in a choice of 16-pin DIP (JN) and 20-terminal PLCC (JP) packages. Price (either package) is $3.35 in 100's, dropping to $2.80 in 1,000s.

ISOLATED LINEARIZED TC-INPUT MODULE

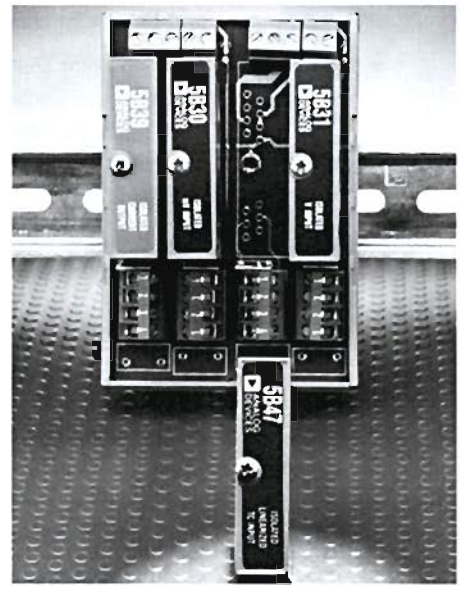
Complete Signal Conditioner with 0.05%-of-Span Accuracy

5B47 Produces 0 to + 5-Volt Outputs from J, K, T, E, R, S, B

The 5B47*, a 2.25" × 2.25" × 0.6" plug-in, accepts thermocouple signals and provides a linear, isolated 0 to +5-V output. Smaller and less costly than other market offerings, it is also competitive with in-house designs.

The 5B Series modular signal-conditioner family was introduced in these pages (20-2, pp. 8-9). 5B's, in modular packages with standard interconnections and ready access to field wiring, interface to transducers, millivolt-level signals, and current inputs.

The input has open-thermocouple detection and 240-volt rms fault protection; an input filter rejects line frequencies (60 dB). Transformer isolation (1.5-kV rms continuous) gives 160-dB CMR. The 5B47 meets IEEE-472 surge-withstand standards.



Cold-junction compensation and chopper-stabilization foster measurement precision. A TTL-driven output switch eases multiplexing. The selectable signal span is ±5 mV to ±0.5 V; accuracy (J & T) is to within ±0.5°C, including nonlinearity, hysteresis, and repeatability errors. Zero and span errors are ±0.05% of span.

The 5B47 operates from −40 to +85°C, requires a single +5-volt supply, and dissipates 150 mW. Price (250s) is $130.

12-BIT, 1-MHz TRACKING ADC IN A DIP

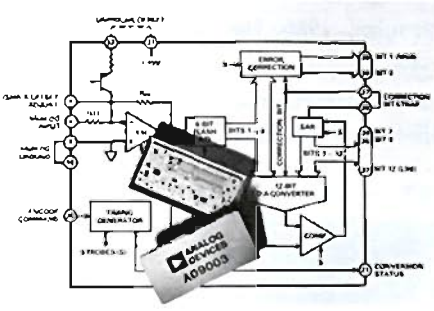
AD9003 Has 850-ns Maximum Conversion Time

No Missing Codes over Full Operating Temperature Range

The AD9003* combines a 12-bit a/d converter and a track-hold amplifier in a single package. Maximum conversion time of 850ns—including acquisition time—insures true 1-MHz performance. Because it is small and completes, the AD9003 is suitable for digital oscilloscopes, high-speed data-acquisition, and radar systems.

Combining an ADC and T/H in the same package permits complete ac and dc characterization of the device; specifications include −74 dB maximum in-band THD, 65-dB minimum SNR, and −87-dB typical two-tone IMD. Accuracy specifications include ±1 LSB max differential nonlinearity, ±1.5 LSB max integral nonlinearity, ±0.2% maximum full-scale gain error, and no missing codes over temperature.

Input voltage range is 5 V p-p. Typical



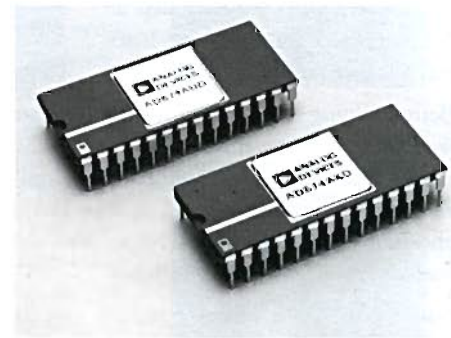
aperture jitter and delay are 26 ps and 16 ns. All digital outputs are TTL-compatible. Coding for the 12-bit parallel output word is complementary binary (unipolar) and complementary offset binary (bipolar).

The AD9003 is packaged in a 40-pin double-width hermetic metal DIP and requires +5V and ±15-volt supplies. Specified operating temperature ranges include 0 to 70°C (KM) and −25 to +100°C (SM and TM). Price in 100s begins at $250.

*Use the reply card for technical data.

15-μs, 12-BIT ADC

AD674A is Complete, Pin-Compatible with AD574A



The AD674A* is a 15-μs, 12-bit a/d converter that offers faster conversion and bus speed than the AD574, while maintaining all of the features and flexibility that made the AD574 an industry standard. The AD674A is compatible (and highly competitive) with existing 674A devices. The complete 12-bit ADC includes a high-precision voltage reference, clock, control logic, and microprocessor interface.

With its 3-state buffers and maximum data-access time of only 150 ns, the AD674A can interface to most digital processors; data is read as one 12-bit word or as two 8-bit bytes. While normally operating under μP control, it can also stand alone.

In addition to its fully specified performance with ±12-volt or ±15-V power supplies (while drawing 390 mW), it furnishes a pin-programmable choice among four calibrated signal ranges, 0 to +10 V or +20 V, and ±5 V or ±10 V. The internal buried-Zener reference has maximum error of 1%; it is trimmed to 10.00 volts, drifts less than 15 ppm (typ), and can drive external loads up to 2.0 mA.

Other key specs include ±1/2-LSB maximum nonlinearity over temperature (K & L grades) and no missing codes over the temperature range. The AD674A is available in six different grades, with performance rated over the 0 to +70°C commercial temperature range (J/K/L) and the −55 to +125°C military range (S/T/U). MIL-STD-883B versions will be available soon. All grades are housed in 28-pin hermetic ceramic DIPs. Pricing starts at $39.25 (100s).

ANALOG DEVICES NAMES THREE NEW FELLOWS

Jody Lapham

Jerome F. Lapham was born in Fort Edwards, NY. He received a BChE in 1960 and a BS in Physics (with distinction) in 1963, both from Clarkson College of Technology, and in 1965 was awarded an MS in Physics from the Case Institute of Technology.

Before joining Analog Devices Semiconductor (ADS) in 1974, he worked at Sprague Electric Company, where he managed a high-speed-TTL line, developed processes, and produced a number of smart power circuits, including dual Darlingtons, power drivers, and high-voltage display drivers—also standard linear products, such as op amps and d/a switches.

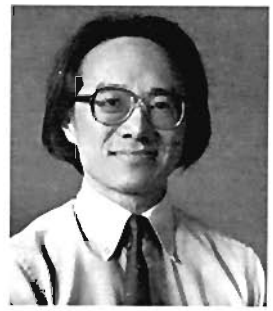
Coming to ADS, he managed all aspects of wafer fabrication, improving yields, designing facilities, developing processes for many high-performance devices, making thin-film resistor process manufacturable, and helping to solve reliability problems. Later, as Wafer Engineering Manager, then Manager of Advanced Wafer Processing, he was involved in BiFET and complementary bipolar development programs, improvement of thin-film-resistor stability and reliability, and establishing a measurement capability for transistor model parameters.

Most recently, as Senior Staff Engineer, he has been deeply involved in perfecting a complementary bipolar (CB) process, which makes possible PNP and NPN transistors with nearly equal capabilities. Products manufactured with this process combine the low drift and high gain already demonstrated in earlier NPN-based products with the wide bandwidth made possible by improved PNP transistors. Examples include the AD568 high-speed DAC (*Analog Dialogue* 21-2), the recently announced AD842, AD845, and AD847 op amps, and many other products to be seen in these pages in future issues.

CB was described in a paper prepared by Jody (jointly with Brad Scharf and Rich Payne) for presentation at the IEEE Bipolar Circuits Conference in Minneapolis MN, September, 1986. He has a number of patents, with more in the works.

Jody lives with his wife and children in Groton, Massachusetts. He enjoys swimming (usually with fellow-Fellow Paul Brokaw) and is an antique-boat enthusiast.

Bob Tsang



Robert W. K. Tsang was born in Shanghai, China. He won a BS-with First Degree Honors in Chemical Engineering at the University of London, in 1958, and received an MS in Chemical Engineering from MIT in 1960.

Upon graduation, he joined Fairchild Semiconductor, in Mountain View, CA, as a Process Engineer, and was promoted to Senior Process Engineer. Later, as Member of the Technical Staff at Sprague Electric Research Center, North Adams MA, he made fundamental contributions to the understanding of the device physics of lateral PNPs; at Zenith Radio, Elk Grove IL, he was Group Leader in monolithic wafer processing.

He joined Analog Devices Semiconductor, in Wilmington MA, in 1972, and—prior to his elevation to Fellow—has served as Group Leader-Process Development, Device Development Manager, Manager of Silicon Device Processing, and Senior Technology and Device Engineer.

His important contributions have resulted in patents and profits. He has been responsible for development of new processes that have made possible many of the devices that appeared in feature articles in this publication and have long since become industry standards.

For example, Bob developed Bipolar Process 2, the I^2L-compatible linear process that is the mainstay of ADS's successive-approximation a/d converter effort. He also invented a diffused buried-Zener technology, for stable, reliable, laser-trimmable references before ion implantation came into wide use. He was also responsible for developing our BiMOS II process; it combines the density of CMOS with the precision of bipolar and makes possible fast, high-accuracy converters. BiMOS II products include the AD569 and 2S80, (seen in recent issues); many more will be available soon.

Bob is married and has two daughters. He enjoys working in the yard and playing tennis.

Mike Tuthill

Before becoming an ADI Fellow, Mike Tuthill was a Staff Engineer for Analog Devices, BV, in Limerick, Ireland—the town of his birth in 1948. He went to school locally and from there to University College (Cork), whence he was graduated in 1970 with a BE (Bachelors of Engineering) degree.

His first job was with Marconi Radar Division in Chelmsford, Essex, England; he worked for 2 1/2 years as a designer of 100-MHz to 4-GHz microwave circuits (with transistors).

He then returned to Ireland to work as a designer of FDM equipment with an Irish telecommunications firm, Telectron. His work embraced a wide variety of circuits from dc to 4 MHz, including amplifiers, crystal oscillators, carrier generators, and frequency multipliers, mixers, etc.

In 1977, back in Limerick, he joined the startup analog CMOS manufacturer, Analog Devices BV, as a Senior Design Engineer; he has since advanced to Staff Engineer—and now, Fellow.

Mike has been responsible for, participated in, or influenced the design of most of ADBV's important CMOS data-conversion products. Examples include: the AD7574 8-bit CMOS ADC, the AD7546 16-bit guaranteed-monotonic DAC, the AD7582/78 12-bit auto-zeroed CMOS ADCs—and most recently, the AD7572 and AD7672 high-speed 12-bit bipolar/CMOS ADCs. His innovations have resulted in a number of patents.

He is married to Marie and has two daughters, Eve (18) and Jean (6). His pastimes include camping and caravanning in Europe, swimming, walking, reading, and—of course—electronics.

WHAT IS AN ADI FELLOW?

ADI Fellows constitute the highest levels of a Parallel Ladder program, started in 1980 and developed to clarify and enhance the career opportunities for technical contributors at Analog Devices. The program is intended to provide the same career potential for technical contributors as for managers, in terms of compensation, recognition, and impact on the corporation. With it, the Company aspires to retain and motivate lifelong career technologists as a cornerstone to continued success.

Analog's program recognizes that technical contributors expand their influence and contributions to the company as they progress in their careers, with contributions equivalent in scope to those of professionals who choose management careers.

An example of the nature of this career potential can be seen in the table, which illustrates the equivalences between technical contributor positions and those of the management hierarchy; below the office of President:

Technical Contributor	Manager
Fellow	VP/General Manager/Director
Senior Staff Engineer	Product-Line Manager
Staff Engineer	Functional Manager
Senior Project Engineer	Engineering Supervisor

Fellows combine many of the following roles: innovator, mentor, entrepreneur, consultant, engineering manager, organizational bridge, teacher, publisher, gatekeeper, and ambassador—in a way that produces an important impact on the corporation.

Nominations for Fellow are initiated by the technical community, spearheaded by the current Fellows. Although many of the earlier Fellows are design engineers, the newest crop includes process engineers—signifying the importance of our technologies in the progress of the company.

In general, according to President Ray Stata, "we are looking for innovation, for past and future contributions, and for people we can look at and say that we want our other technical people to aspire to be like them."

As of today, our Fellows are:

A. Paul Brokaw (1980)
Lew Counts (1984)
Barrie Gilbert (1980)
Peter R. Holloway (1985)
Jody Lapham (1988)
Jack Memishian (1980)
Michael P. Timko (1982)
Robert W. K. Tsang (1988)
Mike Tuthill (1988)

MORE AUTHORS (Continued from page 2)

Jeffrey Greenwald (page 10) is a Design Engineer in the Interface Products Division at Analog Devices in Norwood MA. He earned his BSEE in 1980 from Northeastern University. He is an active member of ISHM and the Audio Engineering Society. In his spare time, he is a musician on home-recording projects and enjoys struggling with his golf game.

Bill Sheppard (page 10) is a Marketing Engineer in the Interface Products Division (IPD) of Analog Devices. Since joining ADI in 1969, he has held positions as Test Supervisor and Quality-Control Supervisor. In his present position, he supports IPD's High-Resolution Converter product line. He received his ASET at Brevard Junior College in Cocoa, Florida. His hobbies include golf, fishing, and high-performance Buicks.

Bob Malone (page 12) is a Design Engineer at the Microelectronics Division of Analog Devices, in Wilmington MA. Before joining the company in 1984, he was a Design Engineer with the Test Systems Division of Fairchild. Bob holds a BSEE from RPI and an MSEE from Northeastern University. In his spare time, Bob enjoys spending time with his family.

Rene Sierra (page 12) is Product Marketing Manager for Signal-Processing Components at ADI's Microelectronics Division. Prior to joining Analog Devices, he worked as a Design Engineer at Hughes Aircraft (Los Angeles) and as a DSP/Converter Marketing Manager at TRW LSI products (San Diego). Rene has a BSEE from the University of Puerto Rico. In his spare time, he enjoys "building things" and playing golf.

Tom Tice (page 18) is an IC Project Engineer on high-speed a/d converter design at ADI's Computer Labs Division. Earlier, he was engaged in instrumentation design at R. J. Reynolds Industries. He received a BSEE from North Carolina State University in 1983. In his spare time, he designs and builds stereo hi-fi equipment and plays golf, racquetball, and volleyball.

Worth Reading

DATABOOKS & SHORT FORMS

Data-Conversion Products Databook and **Linear Products Databook.*** Two volumes (shipped as a unit) containing 2,022 pages of *FREE* technical data on high-performance products for data acquisition and linear signal processing. 23 product classes include op amps (42 families), instrumentation amps, isolators, comparators, analog function circuits, signal conditioners, voltage references, track-holds, and a/d-, d/a-, v/f-, and resolver-digital converters. There are comprehensive data sheets, selection guides, and much other useful information. With the **DSP Products Databook**, described in the last issue, they form a complete three-volume catalog of the world's most-comprehensive line of ICs and other products for high-performance signal processing: digital, analog, and interface.

Analog CMOS Switches and Multiplexers.* A short-form guide to switches and multiplexers manufactured using ADI's LC^{2}MOS (linear-compatible CMOS) high-performance enhanced process featuring high breakdown voltages, low R_{ON}, low leakage, and high stability. 16 pages of product listings, block diagrams, reliability data, and more.

LTS-2020 Series Test Systems. A 45-page short-form guide to LTS-2020-series Component Test Systems for incoming test and inspection, component evaluation, and semiconductor product testing. Described are system consoles; test capabilities for linear and discrete devices, data-conversion devices, and digital devices; as well as prototyping hardware, handlers, options, and supplies. Write to Analog Devices Component Test Systems, 181 Ballardvale St., Wilmington MA 01887 or phone (617) 658-9400.

Revised ADSP-2100 Manuals. Now available, the newly revised **ADSP-2100 User's Manual** describes the ADSP-2100's architecture, and includes an overview of the instruction set. **The ADSP-2100 Cross-Software Manual**, a programmer's reference, has major new information coinciding with Release 1.5 of the Cross Software; complete programming information in one book, it includes a bound-in Reference Card and a chapter devoted to the new C Compiler. Get in touch with the local sales office to request a free copy of either (or both) book(s).

SERIALS

Analog Briefings—*The Newsletter for the Military/Avionics Industry.* Volume IV, No. 1 discusses standard military drawings for the ADSP-2100 DSP µP; addition of ADI's Microelectronics Division to the MIL-STD-1772 *Section B* Qualified Manufacturers List; the meaning of the "B" in our /883B part markings; MIL-STD-883 Notice 5 and 6 changes; issues in new ESD proposals by the U. S. Government; and new military-grade and Standard-Military-Drawing products now available. Also included is a 4-page insert with a recent compilation of our available QPL, SMD, and /883B products. For a free copy, and to subscribe, get in touch with our nearest sales office.

DSPatch—*The Digital Signal Processing Newsletter.* Number 7 (16 pp.) features "Analog Issues for Digital Systems," which will become a regular feature. Also included are articles on uses of Analog Devices DSP chips by Hewlett-Packard (workstation and floating-point accelerator), Loughborough, Hazeltine (systolic processor), and Logabex; Questions & Answers; update on products, data sheets, and support, seminars and training programs, and much more. For a free copy, and to subscribe, get in touch with our nearest sales office.

APPLICATION NOTES

*AD7578 and AD7582 Performance with Reduced V_{DD} Supply (12 V ±10%),** by Dan Sheehan, summarizes performance in 12-volt operation for 100-µs, 12-bit a/d converters, and compares it with the +15-volt data-sheet specifications. 2 pages.

*Circuit Applications of the 2S81 and 2S80 Resolver-to-Digital Converters,** by Hitesh Patel, discusses topics of interest to users of monolithic resolver-to-digital converters, ranging from power-supply connections to incremental encoder simulation and connection to Inductosyns®. 6 pages.

*Dynamic Characteristics of Tracking Converters,** by Mark Thomas, a simple explanation of the dynamic-characteristic specifications, explains their particular relevance for synchro- and resolver-to-digital converters. Especially helpful to designers interested in using the 2S80 and 2S81 monolithic RDCs. 4 pages.

*Dynamic Performance of CMOS DACs in Modem Applications,** by Mike Curtin and Matt Smith, looks at the performance of a number of CMOS DACs when generating a standard carrier frequency for V32 and V33 modems. 6 pages.

*8th-Order Programmable Low-Pass Analog Filter Using Dual 12-Bit DACs,** by Bill Slattery, describes the design of a low-pass analog filter with software-programmable cutoff frequencies, from 100 Hz to 50 kHz, using the AD7537 DAC. 8 pages.

ARTICLE REPRINTS AVAILABLE

"Quad 12-Bit V-out DAC IC Reads Back Input Words to Host,"* *Electronic Design*, December 10, 1987. (AD664).

"Stable Reference IC Simplifies the Design of Analog Systems,"* by Bill Thompson, *EDN*, January 21, 1988. (AD588).

ADI AUTHORS IN THE TRADE PRESS

"Converters Digitize Signals for DSP," by Bob Malone, *EDN News*, January, 1988.

"Programmable-Delay ICs Control System Timing," by Craven Hilton and Jeff Barrow, *EDN*, February 18, 1988. (AD9500).

"Transform Your IBM PC into a 6 1/2-Digit Voltmeter,"* by Geoff Haigh, *Electronic Design*, February 18, 1988. (AD1175).

BRIEF BOOK REVIEW

Operational Amplifier Circuits—Theory and Applications, by E. J. Kennedy. New York: Holt, Rinehart and Winston, Inc., 1988. ISBN 0-03-001948-6. Topics include: The ideal operational amplifier, The non-ideal operational amplifier, Frequency stability for multiple-pole systems, Noise analysis in op-amp circuits, Other linear circuit applications, Active RC filters, Nonlinear and other functional circuits, and Transducers and signal-processing examples; plus 5 Appendixes. Our Contributing Editor, Bill Schweber, comments: "Fairly thorough. Appendixes D (Computer Modelling) and E (R & C tables) were especially useful, as was Chapter 8." [*Not available from Analog Devices.*]

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Potpourri

An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

REVISED DATA SHEETS . . . Data sheets for ADG526A/527A and ADG528A/529A, numbered C1153 and C1041, dated 11/87, have been replaced by C1153a and C1041a, dated 2/88 (see upper RH corner of back pages). In C1041a, incorrect 16-pin outline drawings are replaced by correct 18-pin; and room-temperature specs are corrected to +25°C from -25°C. In C1041a, incorrect truth tables have been replaced and room-temperature is corrected to +25°C . . . A corrected version of the AD7824/7828 data sheet, C950b, dated 5/2/88, is now available . . . A revised version of the ADSP-2100 data sheet, C1064a, dated 1/88, is available. It includes information about the PLCC (PQFP) package and minor revisions to specifications and timing.

PRODUCT NOTES (COMPONENTS) . . . Using or considering the OP-42 or OP-44? You should also consider the AD711 and AD744; Consult your nearby ADI sales office for the 8-page results of a bench evaluation that concludes "Our parts clearly win on ac performance, dc performance, packaging, and price." . . . Op amps available in SOIC packages: ADOP-07CR, AD707JR/KR, AD711JR/KR, AD548JR/KR . . . A low-cost exact plug-in replacement for the Brand "B" 16-bit ADC, the ADADC71JD/KD, is now available. (And it has a wider NMC temperature range—0-70°C vs. 10-40°C) . . . The flood of surface-mountable products continues to crest; among the converter types newly available in PLCC: AD650 and AD574A; in LCC, AD558; and in SO, AD586 . . . Revised specs for ADSP3201/02/10/11/20/21: J/K/S/T only (not including ADSP-3210L/U), t_{SU} is 25 ns, t_{RS} is 75 ns . . . Revised specs for ADSP-1401: I_{DD} (Quiescent Supply Current) is 50 mA (J/K) and 65 mA (S/T); I_{DD} (Supply Current) is 90 mA (J/K), 115 mA (S/T); ITSOV is 13 ns (J/K) and unchanged for S/T . . . AD96685/87: PLCC samples are available . . . AD9502 data sheet: Delete last paragraph (p. 8) . . . Typical distortion measurements on AD9610 transconductance op amp have shown less than -80 dB 2nd & 3rd below 3 MHz and less than -100 dB below 10 kHz (unity-gain inverter, R_L = 100 Ω, V_{OUT} = 2 Vp-p) . . . The AD368 12-bit sampling ADC with programmable gain is similar to the AD369 (*Analog Dialogue* 20-1) but has a series of octal gain steps: 1, 8, 64, 512. Military (SD) versions of both devices are available . . . Rev. 1.5 of ADSP-2100 Cross Software eliminates bugs and adds enhancements. In addition to IBM-PC and VAX/VMS versions, UNIX BSD 4.2 is now available in data cartridges for Sun-2 and Sun-3 workstations. Announcements of these revisions will appear in DSPatch and the DSP Bulletin Board (see "Potpourri" in 21-2) . . . Rev. 3.0 of ADSP-2100 Emulator firmware now available—eliminates bugs; will go to all Emulator customers . . . Evaluation boards are available for flash converters: AD9000, AD9012, AD9002; and for high-speed op amps:AD9610 & AD9611. Consult the sales force.

PRODUCT NOTES (SYSTEMS) . . . Consult the **System Sales force** for information about the following: . . . The µMAC-6000 is now available with an optional 8087 math co-processor . . . Solid-state relays for our relay modules and boards are now being furnished by a different supplier. The new products are UL and CSA approved. A small subset have specs that differ in turn-off time or turn-on current from those of the original modules; they are identified with the suffix, "A" . . . Enhanced µMACBASIC, Rev. 2.20 is being shipped with µMAC-6000M, and Rev. 2.01 on µMAC-6000E. Will handle twice as many Analog Expansion backplanes (4 vs. 2) and Analog I/O points (104 vs. 56); now include MCCOMM and MCCOMM+; and many other enhancements . . . Run-time licenses now available to OEMS/system houses for ASYST. ADI models AC1902 and AC1903; significant discounts in quantity . . . Hotline for IBM PC bus I/O board (RTI-800 Series) inquirers (orders, information, catalogs, etc.): 1-800-4-ANALOG (1-800-426-2564) . . . STB-TC 16-channel signal-conditioning panel for thermocouple inputs to µMAC-6000 and RTI-820—(PC-compatible I/O) . . . Low-cost backplane and I/O options are now available for the µMAC-6000 family.

MILITARY NEWS . . . We are in the process of switching over from hermetic side-brazed ceramic (D) to hermetic Cerdip (O) packages for our CMOS product line. Some newcomer Cerdip families include: AD7501 (J/K/S and SQ/883B), AD7510/11/12DI (J/K/S/T and SQ/TQ/883B), AD7541A (S/T and S/T/883B), and AD7548 (S/T and S/T/883B). PCN customers will receive individual notifications . . . New SMDs: MIL-STD-883B versions of the following generic conversion-product families are now available to Standardized Military Drawings: AD7524 to SMD 5962-87700; AD7528 to SMD 5962-87701; AD7545 to SMD 5962-87702; AD7572 to SMD 5962-87591; AD585 to 5962-87540, AD570; and AD571 to 5962-86802 . . . The AD590 Temperature Transducer is now available to SMD 5962-87571 . . . MIL-STD-883 versions of the AD394 and AD395 quad 12-bit DACs now available; SMDs to come . . . ADLH0032 and ADLH0033 amplifiers now available to DESC drawing 80013 . . . The AD9610 op amp and the AD9000 75-MHz 6-bit flash ADC are now available in MIL-STD-883 versions . . . Reliability reports are available to qualified inquirers for a large number of ADI products; consult the nearest sales engineer. (Recent examples include AD526, AD569, AD586, AD736, AD674 . . . A -55°C to +125°C (SD) version of the 1B31 strain-gage conditioner is now available.

IN THE LAST ISSUE

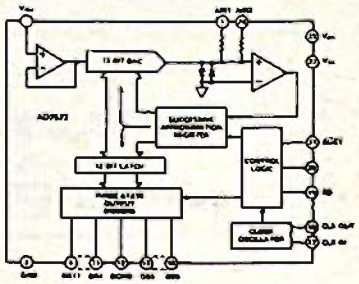
Volume 21, Number 2, 1987 – 32 Pages

ANALOG DEVICES

3μs, 12-Bit Monolithic ADC

AD7672

FEATURES
- 12-Bit Resolution and Accuracy
- Fast Conversion Time
  - AD7672XX03 – 3μs
  - AD7672XX05 – 5μs
  - AD7672XX10 – 10μs
- Unipolar or Bipolar Input Ranges
- Low Power: 110mW
- Fast Bus Access Times: 90ns
- Small, 0.3", 24-Pin Package



AD7672 Functional Block Diagram

PRODUCT DESCRIPTION

The AD7672 is a high-speed 12-bit ADC, fabricated in an advanced, mixed technology, Linear-Compatible CMOS (LC²MOS) process, which combines precision bipolar components with low-power, high-speed CMOS logic. The AD7672 uses an accurate high-speed DAC and comparator in an otherwise conventional successive-approximation loop to achieve conversion times as low as 3μs while dissipating only 110mW of power.

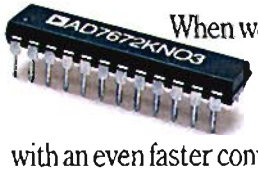
To allow maximum flexibility, the AD7672 is designed for use with an external reference voltage. This allows the user to choose a reference whose performance suits the application, or to drive many AD7672s from a single system reference, since the reference input of the AD7672 is buffered and draws little current. For digital signal processing applications, where absolute accuracy and temperature coefficients may be unimportant a low-cost reference can be used. For maximum precision, the AD7672 can be used with a high-accuracy reference such as the AD588.

The on-chip clock-circuit may be used with a crystal for accurate definition of conversion time. Alternatively the clock input may be driven from an external source such as a microprocessor clock.

PRODUCT HIGHLIGHTS

1. Fast, 3μs, 5μs and 10μs conversion speeds make the AD7672 ideal for a wide range of applications in telecommunications, sonar and radar signal processing or any high-speed data acquisition system.
2. LC²MOS circuitry gives high precision with low power drain (110mW typ).
3. Choice of 0 to +5V, 0 to +10V or ±5V input ranges, accomplished by pin-strapping.
4. Fast, simple, digital interface has a bus access time of 90ns allowing easy connection to most microprocessors.
5. Available in space-saving 24-pin, 0.3" DIP or surface mount package.

AT 5μS, WE SET THE 12-BIT A/D RECORD. THIS PAGE TELLS HOW WE BROKE IT.



When we introduced our AD7572, it set the monolithic 12-bit A/D conversion speed record at 5μs. Now, our AD7672 establishes a new record with an even faster conversion time of only 3μs.

The AD7672 reaches this blazing speed with only 110mW of power dissipation because, like the AD7572, it's manufactured on an advanced merged bipolar/CMOS process.

The 90ns bus access time of the AD7672 affords easy interfacing with most microprocessors, while the +5V and –12V nominal power supply voltages allow its use in PC and modem designs. All this is available in a narrow 0.3" DIP or a surface mount package, so whatever your application, the AD7672 won't take up much space.

The AD7672 also features unipolar or bipolar analog inputs that are selected by pin-strapping. This lets you avoid external circuitry for input range changing.

For more information on how the AD7672 can speed up your designs, contact the Analog Devices office nearest you.

ANALOG DEVICES

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